TECHNICAL INFORMATION

SSI Interface Description

Synchronous Serial Interface for Absolute Encoders

SICK
Sensor Intelligence.

Described product families

AHS/AHM36 SSI

AFS/AFM60 SSI

AFS/AFM60 SSI + Sin/Cos

AFS/AFM60 SSI + Incremental

AFS/AFM60S Pro

ATM60 SSI

ATM90 SSI

ARS60 SSI

TTK70 SSI + Sin/Cos

KH53 SSI

Manufacturer

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Germany

Legal information

Original document

This document is an original document of SICK AG.

1 Introduction

1.1 Absolute encoder

Absolute encoders generate information about position, angle, and rotation counts in type-specific angular steps. A unique code pattern is assigned to each angular step for this purpose. The number of code patterns available per revolution determines the resolution. Each code pattern forms a unique reference, and is therefore an absolute position. There is therefore no need for a reference run after switching on.

1.2 Singleturn/multiturn

A singleturn encoder measures the absolute position within a revolution. A multiturn encoder not only provides the position within a revolution, but also the number of revolutions.

1.3 SSI interface

The SSI interface (SSI = Synchronous Serial Interface) is a communication interface for absolute encoders that is well established in the market. It was originally developed by Max Stegmann GmbH (now SICK) and is used for serial data transmission, which allows absolute positions to be conveyed. The advantage of this method of transmission is that the controller can set not only the time of recording of the position but also the speed of data transmission. The interface is thus an ideal way to ensure reliable data transmission.

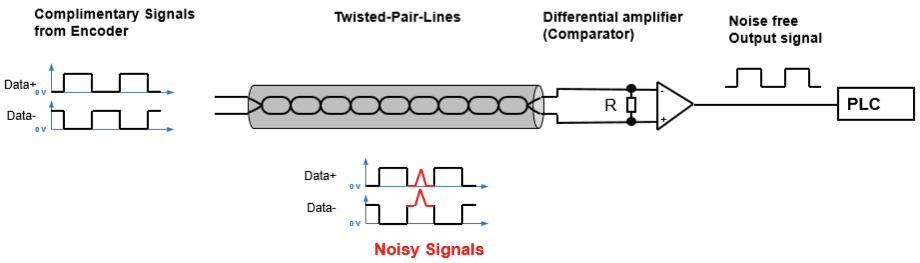
2 SSI interface

2.1 Features of the SSI interface

- Physical basis: RS-422 (EIA 422) or RS-485 (EIA 485).
- Point-to-point connection: Each absolute encoder with an SSI interface requires a connection to an SSI master.
- The data transmission requires four cables (Clock+, Clock-, Data+, Data-).
- The signal cables must be twisted in pairs and shielded.

Figure 1: Twisted pair signal lines

- The SSI master determines the time and speed of the data transmission.
- Baud rates up to 2 MHz are possible (depending on the length of cable).
- Clock and data signals are transmitted and evaluated differentially. This makes the signals less sensitive to EMC interference.



2.2 Sequence of synchronous serial data transmission

- The position is continuously sensed.
- The SSI master requests the position value from the encoder by sending a clock sequence to the clock input of the encoder. (The number of clocks depends on the number of position bits and, if applicable, error bits to be transmitted).
- At the first high-low edge (time 1 in the pulse diagram – see figure 2, page 5), the position value is loaded into the output register.
- At the first low-high edge (time 2 – see figure 2, page 5), the most significant bit of the position value is transmitted to the SSI master.
- At every subsequent low-high edge of the clock sequence, the next lower significant bit is transmitted.
- Once the SSI master has received the least significant bit, it interrupts the clock sequence (time 3 – see figure 2, page 5).
- After the time “tm” (time 4 – see figure 2, page 5), new position values are loaded into the output register inside the encoder.

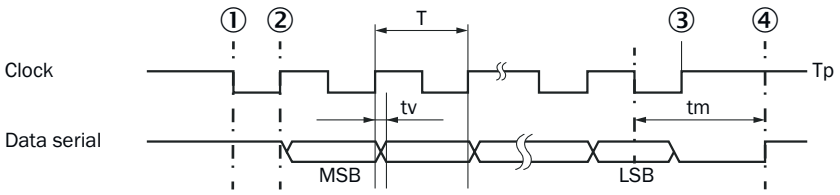


Figure 2: Pulse diagram of data transmission

tv	Delay time for the clock tv < T/2
MSB	Most significant bit
T	Duration of the clock signal
LSB	Least significant bit
tm	Time 15 µs to 25 µs
Tp	Clock interval

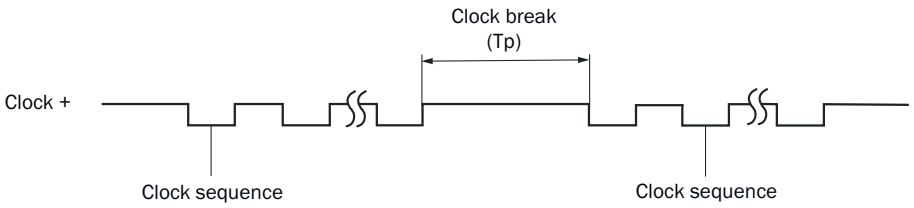


Figure 3: Clock sequences for synchronous serial data transmission - The clock interval is defined by the SSI master and must always be greater than the time tm

2.3 Error bits

In addition to the position bits to be transferred, so called error bits can be transmitted at the end of data transmission. These error bits can be used to transmit various error types from the encoder to the SSI master depending on the absolute encoder product family. The error bits need to then be evaluated in the SSI master or controller.

2.4 The Gray code

Absolute encoders with an SSI interface preferentially use the Gray code. The specific feature of this code is that only one bit changes when transitioning from one position value to the next.

Table 1: Examples of different codes types

Decimal code	Binary code	BCD code	Gray code
0	0000	00000000	0000
1	0001	00000001	0001
2	0010	00000010	0011
3	0011	00000011	0010
4	0100	00000100	0110
5	0101	00000101	0111
6	0110	00000110	0101
7	0111	00000111	0100
8	1000	00001000	1100
9	1001	00001001	1101
10	1010	00010000	1111
11	1011	00010001	1110
12	1100	00010010	1010
13	1101	00010011	1011
14	1110	00010100	1001
15	1111	00010101	1000

Gray excess code

If a suitable section based on the encoder resolution is extracted from the middle of the full Gray code, this gives the so-called Gray excess code (capped Gray code). Using this Gray excess code, it is possible for only a single data bit to change even when the encoder passes through zero despite using a non-binary step count.

2.5 Data formats

The position value can be output in various SSI data formats depending on the absolute encoder product family, e.g., left-aligned, right-aligned, etc. The available data formats per product family are shown in the following sections.

2.6 Additional signals

In addition to transmitting the absolute position via the SSI interface, further generally incremental signals can be output depending on the product family. These are TTL, HTL or sin/cos. Details on how to output these signals depending on the product family can also be found in the following sections.

2.7 Recommended baud rates for data transmission

The baud rate depends on the length of cable. (The cables must be twisted in pairs and shielded.)

Length of cable	Baud rate
m	kHz
< 50	< 400
< 100	< 300
< 200	< 200
< 400	< 100

The position formation time of the encoder used should also be taken into consideration when selecting the baud rate.

2.8 SSI mode

Asynchronous SSI mode:

The position is continuously formed and made available. The time the position is calculated is not related to the clock frequency of the master.

Synchronous SSI mode:

The position formation occurs synchronously to the clock output of the master, i.e., the up-to-dateness of the position value is temporally related to the clock of the master.

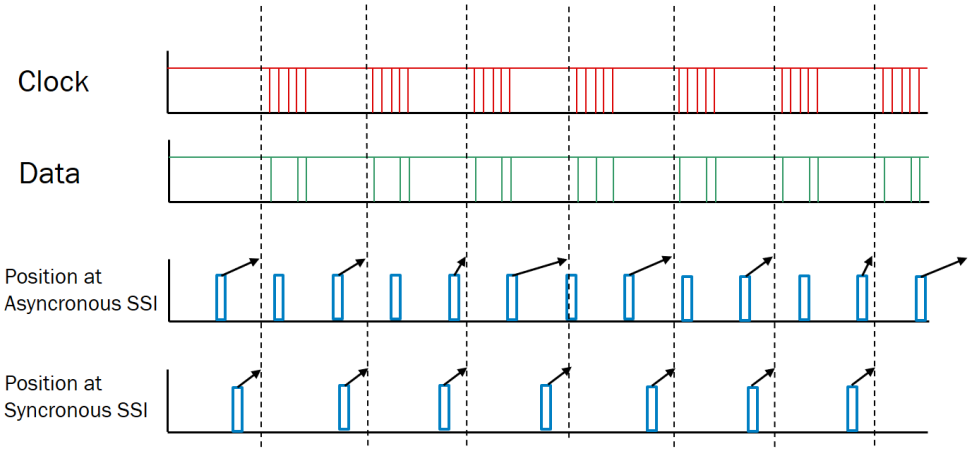
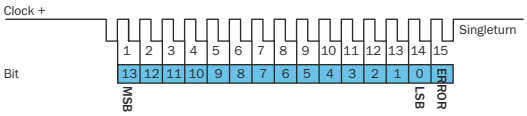


Figure 4: SSI mode

3 Specific features of the SICK encoder product families

3.1 AHS/AHM36 SSI

Singleturn SSI data format



Clock 1–14: Position bits

- LSB: Least significant bit
- MSB: Most significant bit

Clock 15: Error bit

Non-programmable encoder

Non-programmable encoders always output the SSI position MSB-justified (left-justified).

- 14 bits + 1 error bit are always output (irrespective of the type and resolution selected)
- For resolutions below 14 bits, non-assigned bits are filled with 0.

Programmable encoder

- By default, programmable encoders output the SSI position MSB-justified (left-justified).
- Either “binary” or “non-binary” operating mode can be selected to set the resolution.
- All formats (left-justified and right-justified) can be implemented by shifting the bits in the programming interface accordingly using the arrow keys.

Error bit

ERROR: General error. This bit is set as soon as an error occurs in the encoder. This bit remains set as long as the error is present. For non-programmable encoders, the error bit is always output as the 15th bit. For programmable encoders, it can also be output in a “fixed” position as the 15th bit, or transmitted “immediately after” the position bit.

The evaluation of the error bit must be implemented in the controller.

The error bit that is output does not have to be used by the controller. If the error bits cannot be evaluated in the controller, the controller must be set to the encoder resolution. The error bits must then be masked out on the controller side.

SSI mode:

Non-programmable encoders operate in asynchronous SSI mode. In the case of programmable encoders, asynchronous or synchronous SSI mode can be selected in the programming interface. The default setting selected is asynchronous SSI mode.

Asynchronous SSI mode:

The position is continuously formed every 125 µs and made available. The time the position is calculated is not related to the clock frequency of the master. In asynchronous SSI mode, the wait time between two clock pulse trains must be constant in length with a maximum deviation of +/- 20% and must not exceed 600 ms.

When using asynchronous mode, the SSI master must tolerate the same position value being transmitted twice.

Synchronous SSI mode:

The position formation occurs synchronously to the clock output of the master, i.e., the up-to-dateness of the position value is temporally related to the clock of the master. The position formation starts 20 µs after the end of the last clock of a clock pulse train and is then made available after 125 µs. A new position is only formed 20 µs after the end of the subsequent clock pulse train. The wait time between two clock pulse trains must be at least 150 µs.

Programming interface and legend

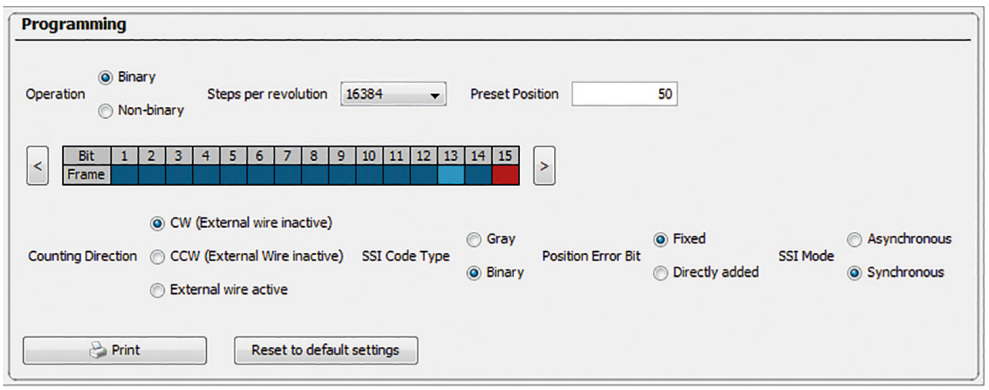


Figure 5: Operating mode: binary

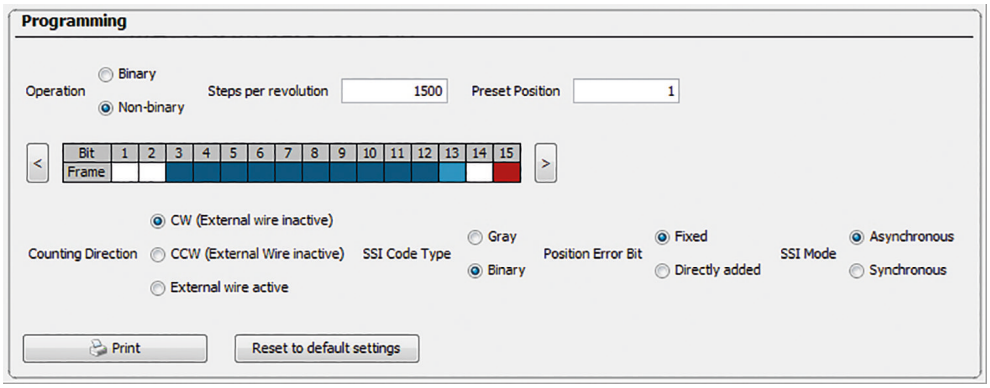
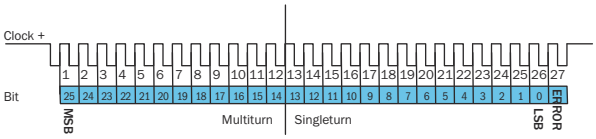


Figure 6: Operating mode: non binary

- -> Error Bit:
  In case of error of the device this bit is set.
- -> Zero Bit:
  At lower resolution, the transmission frame is filled with zero bits.
- -> Position Bits:
  These bits represent the position value, where the value is either Gray-coded or binary-coded. The encoding can be configured via the corresponding input element.

Multiturn SSI data format



Clock 1–12: Multiturn position bits

Clock 13–26: Singleturn position bits

- LSB: Least significant bit
- MSB: Most significant bit

Clock 27: Error bit

Non-programmable encoder

Non-programmable encoders always output the SSI position MSB-justified (left-justified).

- For non-programmable multiturn encoders, the number of revolutions is set to a fixed 4,096 (12 bits).
- 26 bits + 1 error bit are always output (irrespective of the type and resolution selected). For resolutions below 26 bits, non-assigned bits are filled with 0.

Programmable encoder

- By default, programmable encoders output the SSI position MSB-justified (left-justified).
- Either “binary”, “non-binary” or “round axis functionality” operating mode can be selected to set the resolution.
- All formats (left and right-justified, 25-bit mode and Tannenbaum format) can be supported by shifting the bits in the programming interface accordingly using the arrow keys.

Error bit

ERROR: General error. This bit is set as soon as an error occurs in the encoder. This bit remains set as long as the error is present. For non-programmable encoders, the error bit is always output as the 27th bit. For programmable encoders, it can also be output in a “fixed” position as the 27th bit, or transmitted “immediately after” the position bit.

The evaluation of the error bit must be implemented in the controller.

The error bit that is output does not have to be used by the controller. If the error bits cannot be evaluated in the controller, the controller must be set to the encoder resolution. The error bits must then be masked out on the controller side.

SSI mode:

Non-programmable encoders operate in asynchronous SSI mode. In the case of programmable encoders, asynchronous or synchronous SSI mode can be selected in the programming interface. The default setting selected is asynchronous SSI mode.

Asynchronous SSI mode:

The position is continuously formed every 125 µs and made available. The time the position is calculated is not related to the clock frequency of the master. In asynchronous SSI mode, the wait time between two clock pulse trains must be constant in length with a maximum deviation of +/- 20% and must not exceed 600 ms.

When using asynchronous mode, the SSI master must tolerate the same position value being transmitted twice.

Synchronous SSI mode:

The position formation occurs synchronously to the clock output of the master, i.e., the up-to-dateness of the position value is temporally related to the clock of the master. The position formation starts 20 µs after the end of the last clock of a clock pulse train and is then made available after 125 µs. A new position is only formed 20 µs after the end of the subsequent clock pulse train. The wait time between two clock pulse trains must be at least 150 µs.

Round axis functionality

The programmable multiturn encoder supports the gear functions for round axes (endless shaft). Here, the number of revolutions is set as a fraction; a total number of steps is also set. The total number of steps is distributed over the set number of revolutions, e. g., 100 steps for 12.5 revolutions (see example for the programming interface on the next page). The round axis functionality can be used to implement a number for the overall resolution that is not a 2n multiple of the number of steps per revolution. It is also possible to set a non-integer number both for the number of revolutions and for the number of steps per revolution.

Programming interface and legend

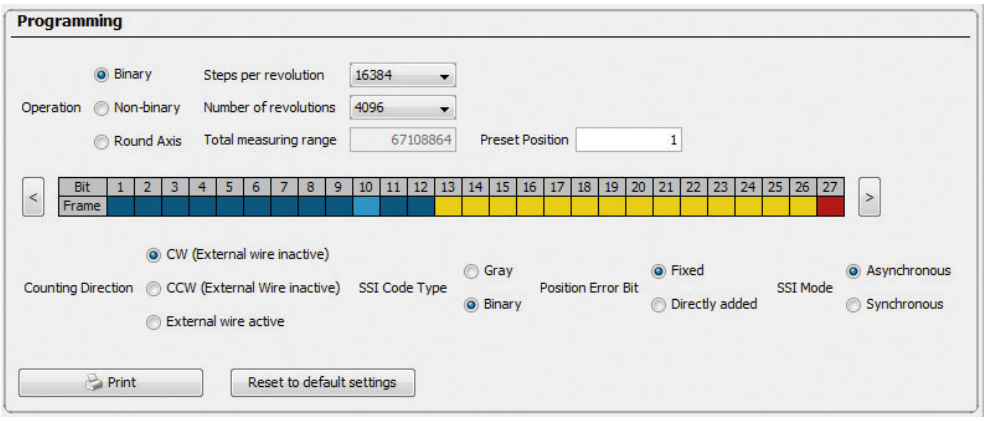


Figure 7: Operating mode: binary

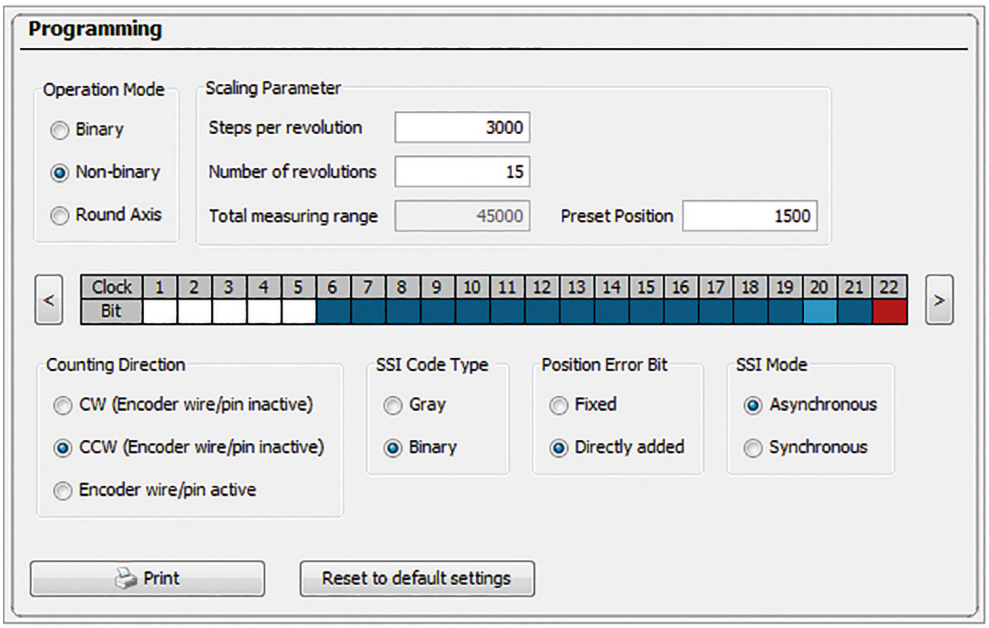


Figure 8: Operating mode: non binary

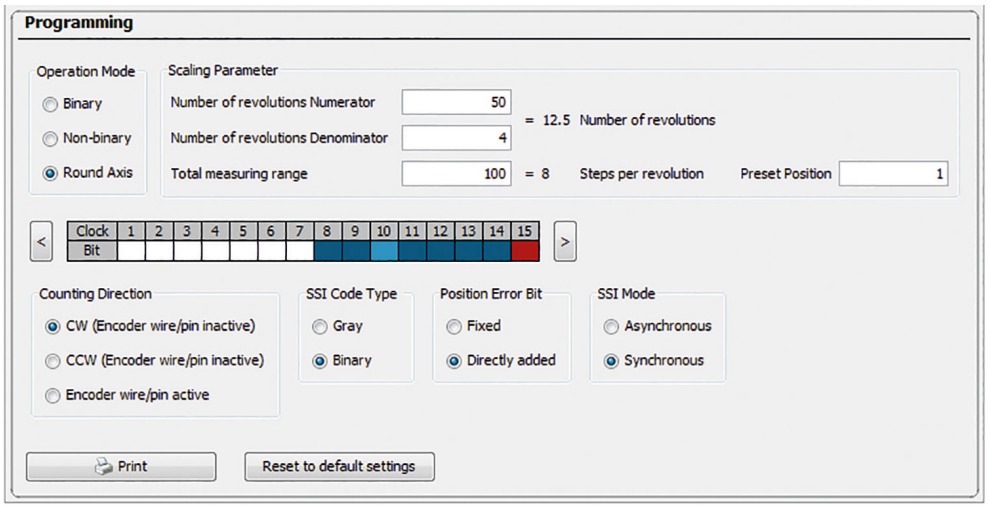
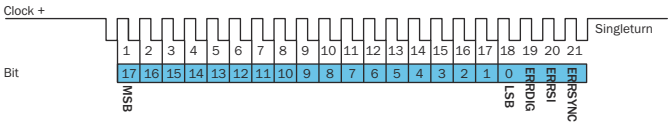


Figure 9: Operating mode: round axis

- -> Multi Bits:
  These bits contain the number of revolutions.
- -> Single Bits:
  In binary operating mode, the multiposition is transmitted separately from the single position. These bits represent the single position.
- -> Error Bit:
  In the event of a device error, this bit is set.
- -> Zero Bit:
  At lower resolution, the transmission frame is filled with zero bits.
- -> Position Bits:
  These bits represent the position value, where the value is either Gray-coded or binary-coded. The encoding can be configured via the corresponding input element.

3.2 AFS/AFM60 SSI

Singleturn SSI data format



Clock 1–18: Position bits

- LSB: Least significant bit
- MSB: Most significant bit

Clock 19–21: Error bits

- ERRDIG: Speed related error message. If this error occurs during the position formation procedure, this is indicated by the ERRDIG bit.
- ERRSI: Error at the light source.
- ERRSYNC: Contamination of the code disk or the reading system. While determining the position, an error arose since the last SSI data transmission. The error bit is cleared during the next data transmission.

The evaluation of the error bits must be implemented in the controller.

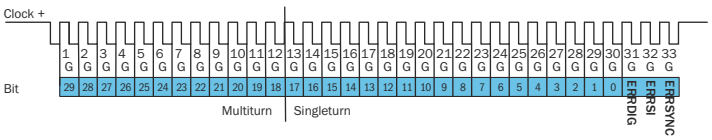
The error bits that are output do not have to be used by the controller.

Example

If the absolute value encoder is set to a resolution of 13 bits, then 16 bits are output: 13 data bits and 3 error bits. If the error bits cannot be evaluated in the PLC, the controller must be set to an encoder resolution of 13 bits. The error bits must then be masked out on the controller side.

Multiturn SSI data format

30 bits



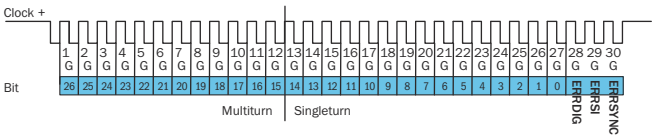
Clock 1–12: Multiturn position bits

Clock 13–30: Singleturn position bits

- LSB: Least significant bit
- MSB: Most significant bit

Clock 31–33: Error bits

27 Bits



Clock 1–12: Multiturn position bits

Clock 13–27: Singleturn position bits

- LSB: Least significant bit
- MSB: Most significant bit

Clock 28–30: Error bits

Error bits

- ERRDIG: Speed related error message. If this error occurs during the position formation procedure, this is indicated by the ERRDIG bit.
- ERRSI: Error at the light source.
- ERRSYNC: Contamination of the code disk or the reading system. While determining the position, an error arose since the last SSI data transmission. The error bit is cleared during the next data transmission.

The evaluation of the error bits must be implemented in the controller.

The error bits that are output do not have to be used by the controller. The multiturn resolution is fixed at 12 bits.

Example

If the absolute value encoder is set to a resolution of 27 bits, then 30 bits are output: 27 data bits and 3 error bits.

If the error bits cannot be evaluated in the controller, the controller must be set to an encoder resolution of 27 bits. The error bits must then be masked out on the controller side.

Additional incremental interfaces

Electrical interface sinus 0.5 V_{SS}

Supply voltage	Output
4.5 ... 5.5 V	Sine 0.5 V_{PP}

Signals before difference calculation at 120 Ω load and at U_S = 5 V

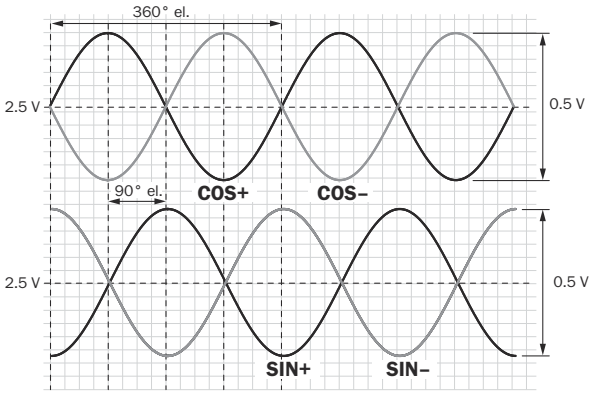


Figure 10: Signal diagram for clockwise shaft rotation looking in the direction “A” (shaft)

Interface signals Sin, Sin-, Cos, Cos-	Signals before difference calculation at 120 Ω load	Signal offset
Differential analog	0.5 V_{PP} ± 20%	2.5 V ± 10%

Signals after difference calculation at 120 Ω load and at U_S = 5 V

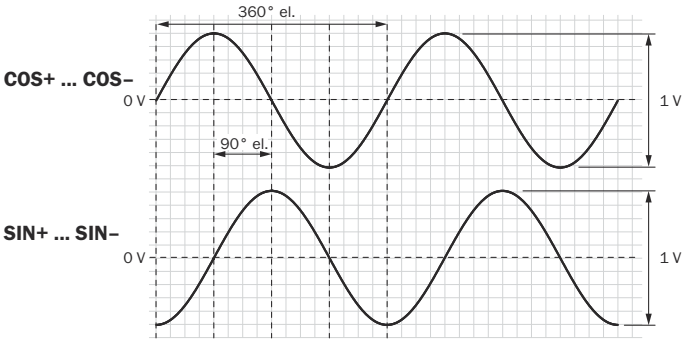


Figure 11: Signal diagram for clockwise shaft rotation looking in the direction “A” (shaft)

Electrical interfaces TTL / HTL

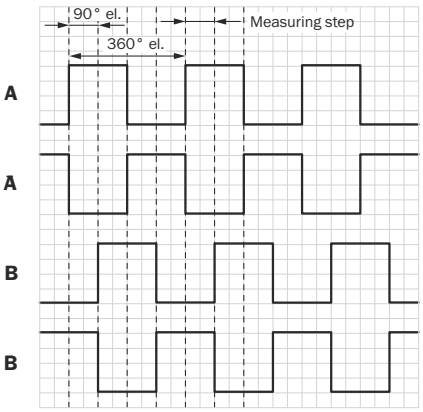


Figure 12: Incremental signal outputs for clockwise shaft rotation looking in the direction “A”, see dimensional drawing

3.3 AFS/AFM60S Pro

NOTE

The AFS/AFM60S Pro is a safety encoder. The information provided below is only an extract from the operating instructions. The primary document for commissioning and use of the AFS/AFM60S Pro is the operating instructions (8025685).

Interfaces

The safety encoder is equipped with an SSI+SinCos interface. The combination of the synchronous serial interface (SSI) with the sine-shaped analog output (SinCos) makes it possible to transmit both absolute position data and speed information.

Singleturn SSI data format

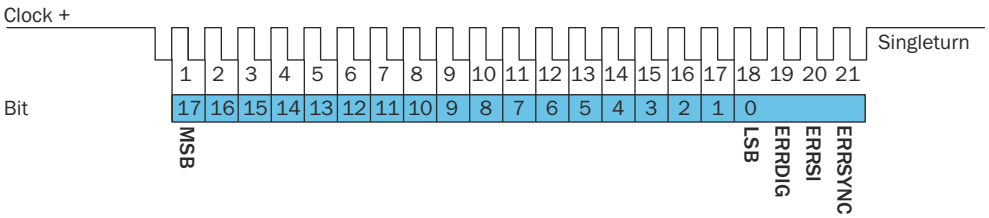


Figure 13: Process data channel 2, SSI data format singleturn, 18 bits

Bit 1-18: Position bits

- LSB: Least significant bit
- MSB: Most significant bit

Bit 1-21 = HIGH: Send "1"

Bit 19-21: Error bits

Error bits

- ERRDIG: Speed related error message. If this error occurs during the position formation procedure, this is indicated by the ERRDIG bit.
- ERRSI: Error at the light source.
- ERRSYNC: Contamination of the code disk or the reading system. While determining the position, an error arose since the last SSI data transmission. The error bit is cleared during the next data transmission.

An internal monitoring system continuously tests the function of the safety encoder. If an encoder detects an error, the error status is displayed to the evaluation system by the SSI channel only outputting "1", whereby the error bits are set.

NOTE

The evaluation of at least one error bit must be realized in the control.

If the safety encoder is set to a resolution of 13 bits, 16 bits, 13 data bits and 3 error bits are output.

Multiturn SSI data format

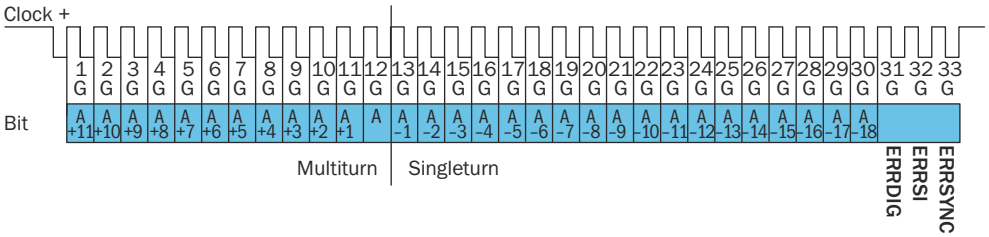


Figure 14: Process data channel 2, SSI data format multiturn, 30 bits

Bit 1–30: Position bits

- Bit 1-12: Multiturn position bits
- Bit 13-30: Singleturn position bits

Bit 1-33 = HIGH: Send "1"

Bit 31-33: Error bits

Error bits

- ERRDIG: Speed related error message. If this error occurs during the position formation procedure, this is indicated by the ERRDIG bit.
- ERRSI: Error at the light source.
- ERRSYNC: Contamination of the code disk or the reading system. While determining the position, an error arose since the last SSI data transmission. The error bit is cleared during the next data transmission.

An internal monitoring system continuously tests the function of the safety encoder. If an encoder detects an error, the error status is displayed to the evaluation system by the SSI channel only outputting "1", whereby the error bits are set.

NOTE

The evaluation of at least one error bit must be realized in the control. 3 error bits are also sent along and should be considered in the control configuration.

The resolution of the multiturn is permanently set to 12 bits.

If the safety encoder is set to a resolution of 25 bits, 28 bits, 12 multiturn data bits, 13 singleturn data bits and 3 error bits are output.

Additional sin/cos interface

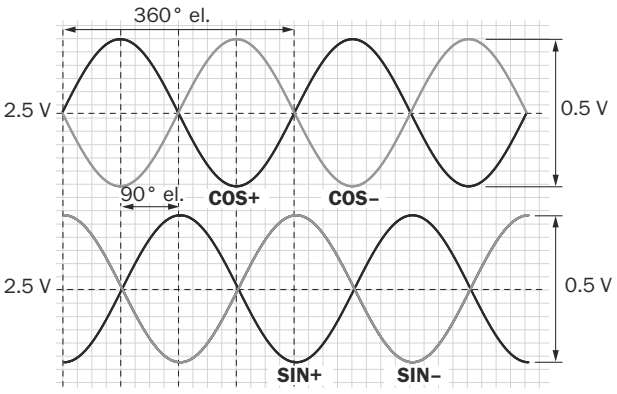


Figure 15: Process data channel 1, signals before difference generation at 120 ohm load. Signal diagram for clockwise (CW) shaft rotation, looking in direction of the shaft

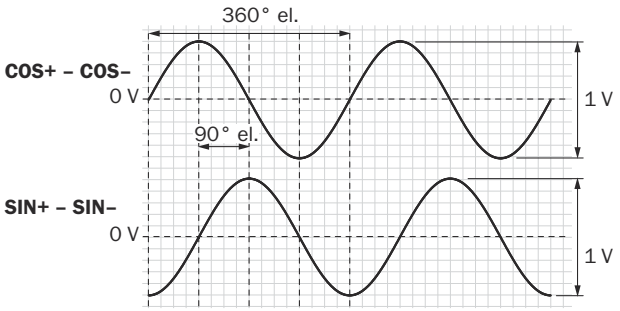


Figure 16: Process data channel 1, signals after difference generation at 120 ohm load. Signal diagram for clockwise (CW) shaft rotation, looking in direction of the shaft

3.4 ATM60 / ATM90 SSI

Multiturn SSI data format

25 position bits in total can be output: 12 bits multiturn and 13 bits singleturn or 13 bits multiturn and 12 bits singleturn.

The so called Tannenbaum format for transmitting the position is permanently set. This means that when a lower resolution is set, the MSB or LSB side is filled with “0” (see graphic).

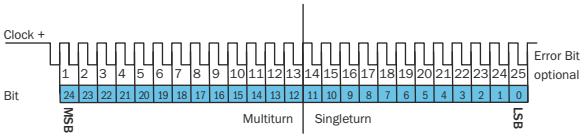


Figure 17: Example: 13 bits multiturn and 12 bits singleturn

Clock 1–13: Multiturn position bits

Clock 14–25: Singleturn position bits

- LSB: Least significant bit
- MSB: Most significant bit

Clock 26: Optional error bit

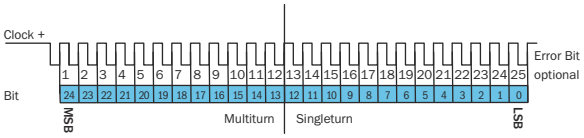


Figure 18: Example: 12 bits multiturn and 13 bits singleturn

Clock 1–12: Multiturn position bits

Clock 13–25: Singleturn position bits

- LSB: Least significant bit
- MSB: Most significant bit

Clock 26: Optional error bit

SSI–RIGHT–ALIGNED

By default, the SSI data are output in Tannenbaum format during standard operation (binary resolution). If this function is enabled, the SSI data area right aligned on the 24th bit. If the “SSI-SHIFT- RIGHT” function is also enabled, the SSI data are right aligned on the 25th bit. This function is not used in round axis operation. Example:

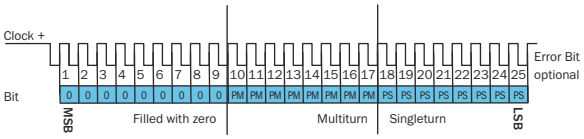


Figure 19: SSI bit structure with 8 bits singleturn and 8 bits multiturn → right aligned

PM	Multiturn position bit
PS	Singleturn position bit

SSI–SHIFT-RIGHT

If this function is enabled, the SSI data are output shifted one position to the right, i.e., the LSB is lost and bit 24 (MSB) is set to logical 0. This applies to all resolution types that are set. Example:

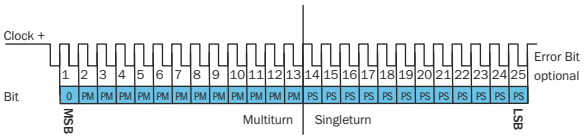


Figure 20: SSI bit structure with 13 bits singleturn and 12 bits multiturn → shift right

PM	Multiturn position bit
PS	Singleturn position bit

SSI mode

Asynchronous SSI mode

During standard operation, the ATM60 forms a position value cyclically every 0.15 ms regardless of the SSI master clock frequency and places this value in the output register provided where it can be fetched through the interface. For a non-binary resolution or round axis functionality, the position formation takes 0.2 ms. Since the SSI clock frequency and the position formation cycle can never be the same, the temporal position assignment will be continuously shifted. In this operating mode, the temporal assignment of the position value varies between 0.005 and 0.15 ms or, for round axis operation, between 0.005 and 0.2 ms.

Synchronous SSI mode

In this operating mode, the recording of the position starts from the first falling edge of the SSI clock, and the position recorded at the last clock pulse chain is sent. This means that the temporal assignment can be determined. For synchronous SSI operation with the standard resolution (no round axis and not a non-binary resolution), the monoflop time tm is fixed at 150 µs. For round axis operation and a non-binary resolution, the monoflop time tm is 200 µs. The recording of the position starts from the first falling edge of the SSI clock and is placed in the output register before the monoflop time tm elapses. The maximum allowed clock frequency in synchronous SSI operation taking into consideration the length of cable is 1.5 MHz. The interval between the clock pulse trains, which needs to be selected on the controller side, is therefore > 150 µs or, when round axis functionality is enabled for a non-binary resolution, > 200 µs.

Round axis functionality

When non-binary resolutions are used, these are represented internally using the round axis functionality. The output format is that required for round axis operation, i.e., only a right aligned output on the 24th bit (bit shift right=0) or the 25th bit (bit shift right=1) can be selected. The various code types such as binary, Gray or Gray excess can be set for this.

The round axis concept encompasses two functions:

1 Non-binary resolutions can be set (specific step count per revolution)
2 A total step count for a configurable physical measuring distance can be selected.

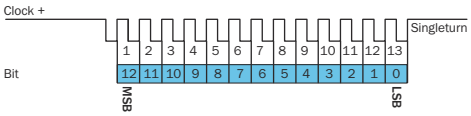
The encoder then starts counting from Zero again (continuous function).

When round axis functionality is enabled, the maximum resolution is based on 8,192 steps x 4,096 revolutions. The physical measuring distance is entered as a fraction, whereby the numerator is a limited to a maximum value of 4,096. The denominator can be set to the value 16,777,216, whereby the maximum encoder resolution of 8,192 steps per revolution cannot be exceeded. This relationship also determines the total step count, which can be set to a maximum value of 33,554,432.

3.5 ARS60 SSI

Singleturn SSI data format

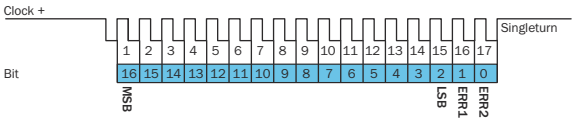
Data format for resolutions ≤ 8,192 steps



Clock 1–13: Singleturn position bits

- LSB: Least significant bit
- MSB: Most significant bit

Data format for > 8,192 steps



Clock 1–15: Singleturn position bits

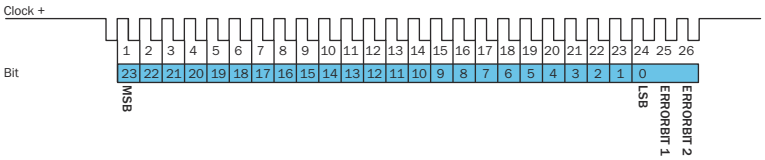
- LSB: Least significant bit
- MSB: Most significant bit

Clock 16-17: Error bits

- Error bit 1: Position error: While monitoring the position, an error arose since the last SSI data transmission. The error bit is cleared at the next SSI transmission.
- Error bit 2: Sender monitoring

3.6 TTK70 SSI

SSI data format



Clock 1–24: Position bits

- LSB: Least significant bit
- MSB: Most significant bit

Clock 25–26: Error bits

- ERROR BIT 1: Error message regarding the distance between the read head and magnetic tape. This bit is set in the SSI data stream if the maximum permitted distance between the read head and the magnetic tape is exceeded. The output position value is invalid.
- ERROR BIT 2: Error message regarding the operating temperature. This bit is set in the SSI data stream if the sensor is being operated above its maximum permitted operating temperature.

The evaluation of the error bits must be implemented in the controller.

The error bits that are output do not have to be used by the controller. To be able to evaluate the error bits, the controller must send at least 26 clock pulses per clock pulse train. A maximum of 31 clock pulses must not be exceeded. If more than 26 pulses are sent, the additional bits are output with "0". If the error bits cannot be evaluated in the PLC, the controller must be set to an encoder resolution of 24 bits.

Sin/Cos interface

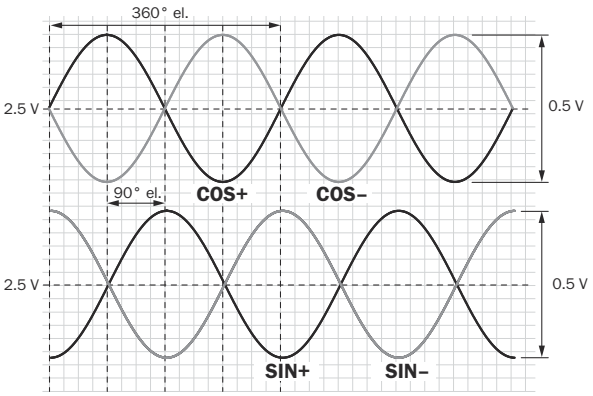


Figure 21: Interface signals before differential generation

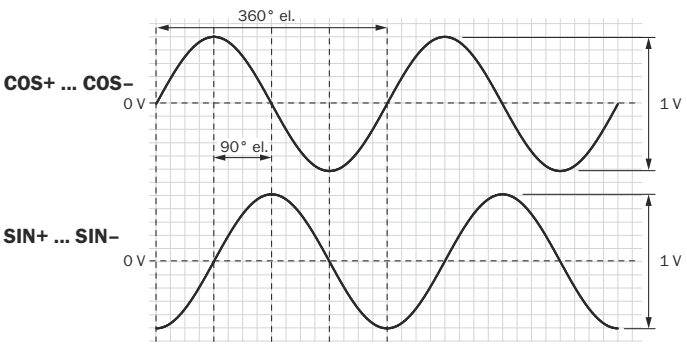
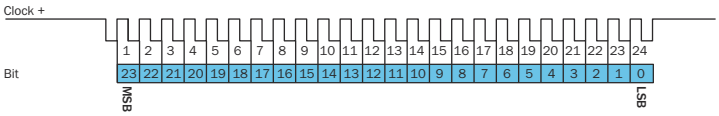


Figure 22: Interface signals after differential generation

Signal	Interface signals	Interface signal for difference calculation at 120 Ω load	Signal offset	Supply voltage	Output
+ SIN - SIN + COS - COS	Analog, differential	0.5 V_{SS} ± 10%	2.5 V ± 5%	4.5 V ... 30 V	Sine 0.5 V_{PP}

3.7 KH53 SSI

SSI data format



Clock 1–24: Position bits

- MSB: Most significant bit
- LSB: Least significant bit

The KH53 SSI has no defined error bits via the SSI data format. If the max. traversing speed is exceeded or the distance between the measuring element and read head is too large, however, the corresponding error message is triggered: FFFFFE Hex.

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