CLOVER DISPLAY LTD.

LCD MODULE SPECIFICATION

Model: CV320240F - _ _ - _ _ - _ _ - _

Revision	08
Engineering	Longson Yeung
Date	27 June 2013
Our Reference	4947

ADDRESS : 1st FLOOR, EFFICIENCY HOUSE, 35 TAI YAU STREET, SAN PO KONG, KOWLOON, HONG KONG.

TEL : (852) 2341 3238 (SALES OFFICE) (852) 2342 8228 (GENERAL OFFICE)

FAX : (852) 2357 4237 (SALES OFFICE)

E-MAIL : cdl@cloverdisplay.com

URL : http://www.cloverdisplay.com

MODE OF DISPLAY

Display mode	**Display condition**	**Viewing direction**
STN : ☐ Yellow green	☐ Reflective type	☐ 6 O' clock
☐ Grey	☐ Transflective type	☐ 12 O' clock
☐ Blue (negative)	☐ Transmissive type	☐ 3 O' clock
☐ FSTN positive	☐ Others	☐ 9 O' clock
☐ FSTN negative		

LCD MODULE NUMBER NOTATION:

CV320240F- MY - S F - N 6 – T
(1) (2)(3) (4) (5) (6) (7) (8)

*(1)---Model number of standard LCD Modules
*(2)---Backlight type
N – No backlight
E – EL backlight
L – Side-lited LED backlight
M– Array LED backlight
C – CCFL
*(3)---Backlight color
N – No backlight
A – Amber
B – Blue
O– Orange
W–White
Y – Yellow green
*(4)---Display mode
T – TN
V – TN (Negative)
S – STN Yellow green
G – STN Grey
B – STN Blue (Negative)
F – FSTN
N – FSTN (Negative)
*(5)---Rear polarizer type
R – Reflective
F – Transflective
T – Transmissive
*(6)---Temperature range
N – Normal
W– Extended
*(7)---Viewing direction
6 – 6 O'clock
2 – 12 O'clock
3 – 3 O'clock
9 – 9 O'clock
*(8)---Special code for other requirements
(Can be omitted if not used)
T – Touch panel (Analog)
P – Touch panel (Digital)

GENERAL DESCRIPTION

Display mode : 320 x 240 dots, graphic TAB LCD module

Interface : 4-bit or 8-bit parallel

Driving method : 1/240 duty, 1/15 bias

Backlight : Side-lited LED

Controller IC : RAIO RA8803 or equivalent
For the detailed information, please refer to the IC specifications.

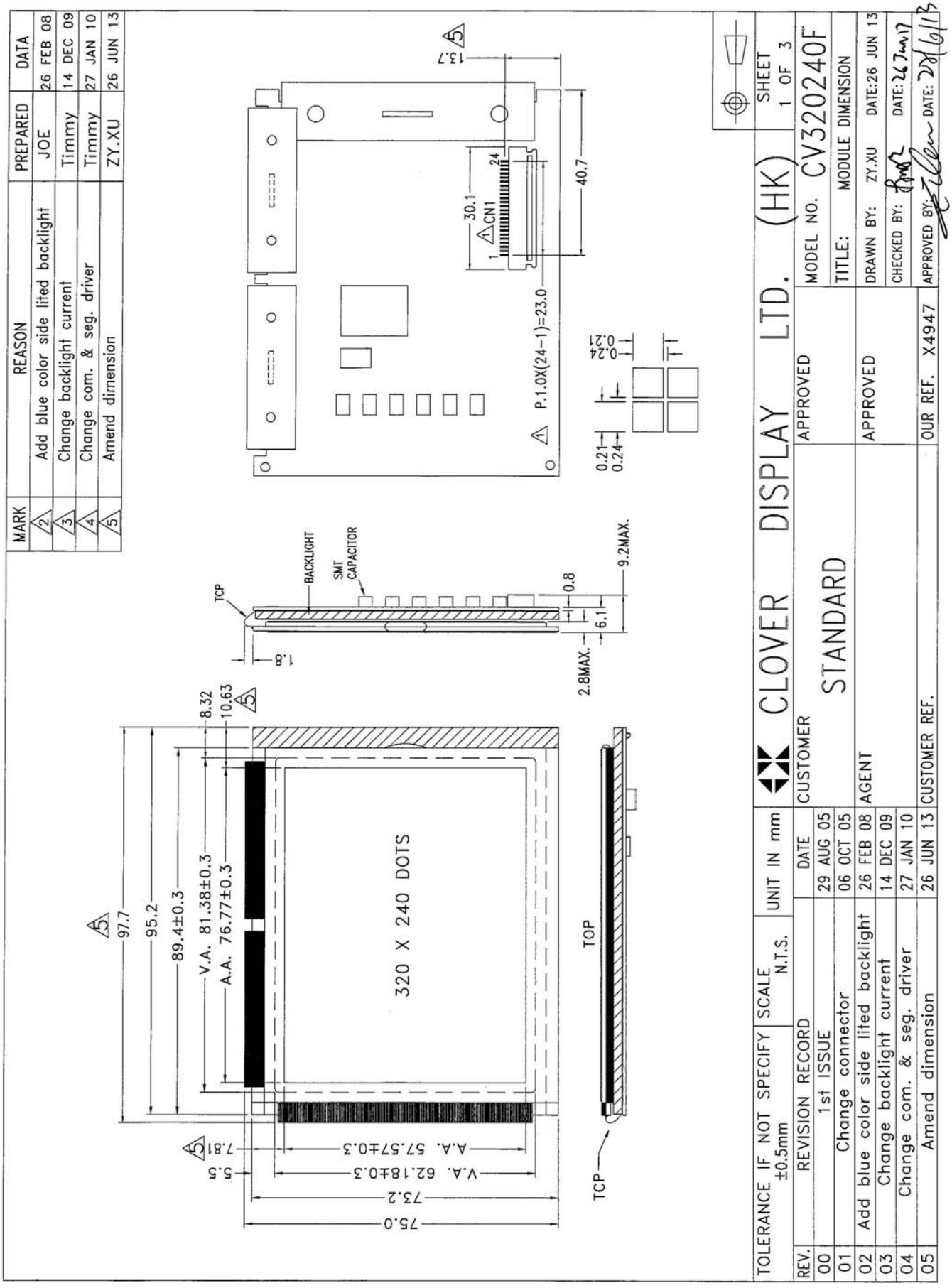
MECHANICAL DIMENSIONS

Item	Dimension	Unit	Item	Dimension	Unit
Outline Dimension	97.7(L)x75.0(W)x9.0(MAX.)(H)	mm	Dot Pitch	0.24(L)x0.24(W)	mm
Viewing Area	81.38(L)x62.18(W)	mm	Dot Size	0.21(L)x0.21(W)	mm

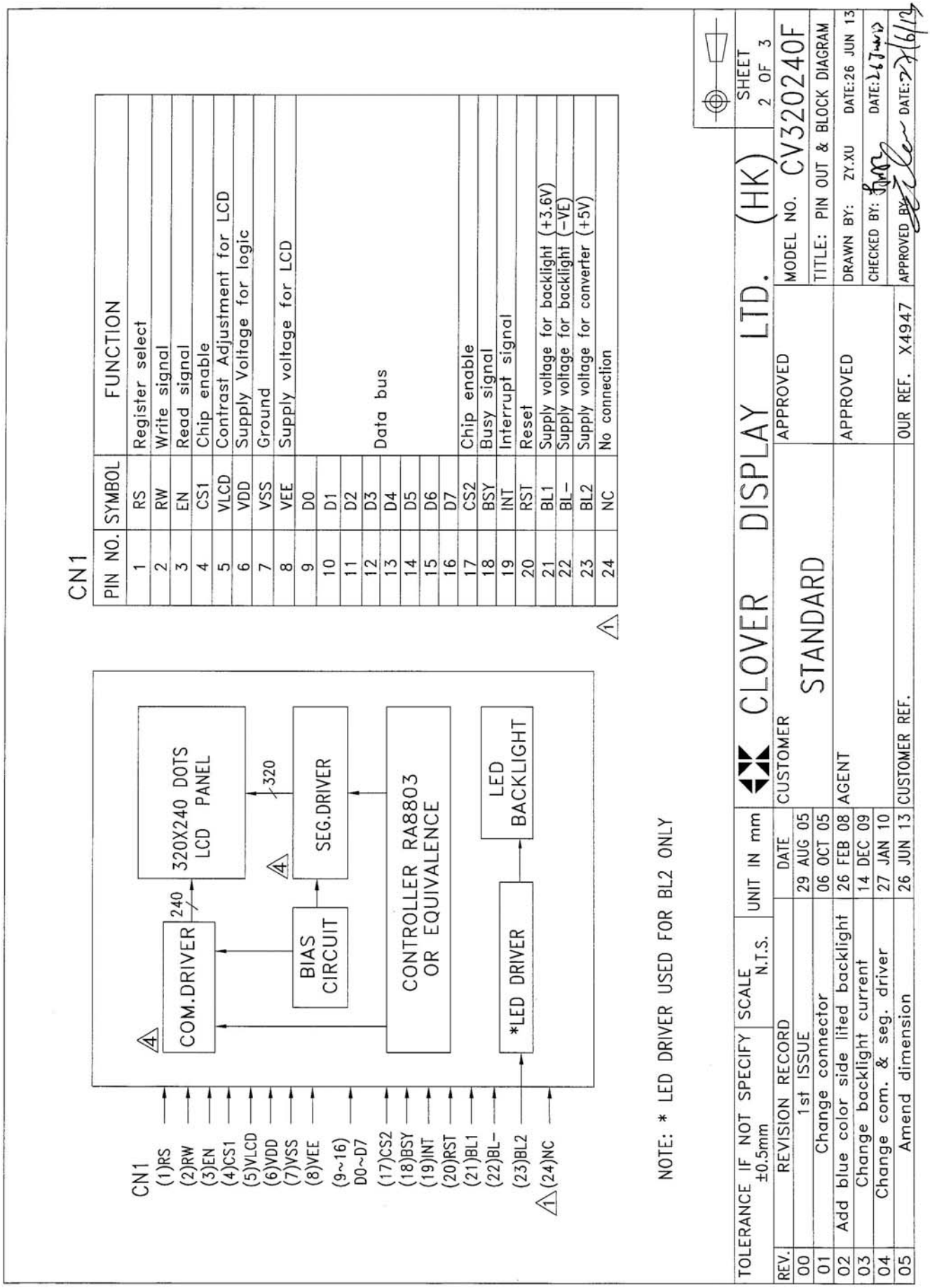
CONNECTOR PIN ASSIGNMENT (CN1)

Pin No.	Symbol	Function
1	RS	Register select
2	RW	Write signal
3	EN	Read signal
4	CS1	Chip enable
5	VLCD	Contrast adjustment for LCD
6	VDD	Supply voltage for logic
7	VSS	Power supply (ground)
8	VEE	Supply voltage for LCD
9	D0	Data bus
10	D1	
11	D2	
12	D3	
13	D4	
14	D5	
15	D6	
16	D7	
17	CS2	Chip enable
18	BSY	Busy signal
19	INT	Interrupt signal
20	RST	Reset
21	BL1	Power supply for backlight (+3.6V)
22	BL-	Power supply for backlight (-VE)
23	BL2	Power supply for converter (+5V)
24	NC	No connection

COUNTER DRAWING OF MODULE DIMENSION



COUNTER DRAWING OF PIN OUT & BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Conditions: VSS=0V, Ta=25℃

Item	Symbol	MIN.	TYP.	MAX.	Unit	Item	Symbol	MIN.	TYP.	MAX.	Unit
FOR SUPPLY VOLTAGE = 5V											
Supply Voltage for Logic	VDD	4.75	5.0	5.25	V	Input Voltage for LCD	VEE	25.0	–	30.0	V
Supply Current for Logic	IDD	–	3.0	6.0	mA	"H"Level Input Voltage	VIH	0.8VDD	–	VDD	V
Contrast adjustment for LCD(*)	VLCD	22.8	24.0	25.2	V	"L"Level Input Voltage	VIL	VSS	–	0.2VDD	V
FOR SUPPLY VOLTAGE = 3.3V											
Supply Voltage for Logic	VDD	3.05	3.3	3.55	V	Input Voltage for LCD	VEE	25.0	–	30.0	V
Supply Current for Logic	IDD	–	3.0	6.0	mA	"H"Level Input Voltage	VIH	0.8VDD	–	VDD	V
Contrast adjustment for LCD(*)	VLCD	22.8	24.0	25.2	V	"L"Level Input Voltage	VIL	VSS	–	0.2VDD	V

Note (*): There is tolerance in optimum LCD driving voltage during production and it will be within the specified range.

Side-lited LED Backlight Forward Voltage (VF)

Constant voltage driving:

Item	Symbol	MIN.	TYP.	MAX.	Unit	Condition
White Backlight current	IBL	–	102	108	mA	VBL = 3.6V
Blue Backlight current	IBL	–	102	108	mA	VBL = 3.6V

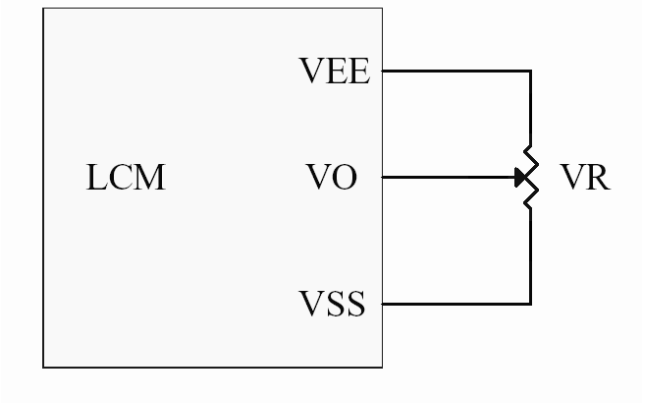
ABSOLUTE MAXIMUM RATINGS

Please make sure not to exceed the following maximum rating values under the worst application conditions.

Item	Symbol	Rating (for normal temperature)	Rating (for wide temperature)	Unit
Supply Voltage for Logic	VDD	-0.3 to 6.5	-0.3 to 6.5	V
Input Voltage for Logic	VIN	-0.3 to VDD+0.3	-0.3 to VDD+0.3	V
Operating Temperature	Topr	0 to 50	-20 to 70	℃
Storage Temperature	Tstg	-10 to 60	-30 to 80	℃

APPLICATION EXAMPLE

A variable resistor is used to adjusting the contrast of the LCD.



Recommend : VR > 50KΩ .

REGISTER LIST TABLE

Reg. No	Reg. Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Default Data
00h	WLCR	R/W	PW1	PW0	SR	--	CG	DP	DK	DV	C9h
01h	MISC	R/W	--	CKN	--	PLR	--	--	CKB1	CKB0	F0h
02h	APSR	R/W	--	--	SP1	SP0	OAR	--	SRFS	--	10h
03h	ADSR	R/W	--	--	--	--	DADR	AUCM	AUSG	SGCM	80h
10h	WCCR	R/W	ARI	ALG	WDI	WBC	AWI	CP	CK	CSD	6Fh
11h	DWLR	R/W	CR3	CR2	CR1	CR0	DY3	DY2	DY1	DY0	22h
12h	MAMR	R/W	GIM	RM2	RM1	RM0	OP1	OP2	WM1	WM0	91h
20h	AWRR	R/W	--	--	X5	X4	X3	X2	X1	X0	27h
21h	DWRR	R/W	--	--	A5	A4	A3	A2	A1	A0	27h
30h	AWBR	R/W	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0	EFh
31h	DWBR	R/W	B7	B6	B5	B4	B3	B2	B1	B0	EFh
40h	AWLR	R/W	--	--	SS5	SS4	SS3	SS2	SS1	SS0	00h
41h	DWLR	R/W	--	--	C5	C4	C3	C2	C1	C0	00h
50h	AWTR	R/W	SC7	SC6	SC5	SC4	SC3	SC2	SC1	SC0	00h
51h	DWTR	R/W	D7	D6	D5	D4	D3	D2	D1	D0	00h
60h	CPXR	R/W	--	--	RS5	RS4	RS3	RS2	RS1	RS0	00h
61h	BGSG	R/W	--	--	DS5	DS4	DS3	DS2	DS1	DS0	00h
70h	CPYR	R/W	RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0	00g
71h	BGCM	R/W	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0	00h
72h	EDCM	R/W	CD7	CD6	CD5	CD4	CD3	CD2	CD1	CD0	EFh
80h	BTMR	R/W	BT7	BT6	BT5	BT4	BT3	BT2	BT1	BT0	33h
81h	FRCA	R/W	--	--	--	--	--	--	--	--	00h
90h	SCCR	R/W	CK7	CK6	CK5	CK4	CK3	CK2	CK1	CK0	04h
91h	FRCB	R/W	--	--	--	--	--	--	--	--	00h
A0h	INTR	R/W	INK	INT	INX	INY	MSK	MST	MSX	MSY	00h
A1h	KSCR	R/W	KEN	KSZ	KDT1	KDT0	--	KF2	KF1	KF0	00h
A2h	KSDR	RO	KS7	KS6	KS5	KS4	KS3	KS2	KS1	KS0	00h
A3h	KSER	RO	KD7	KD6	KD5	KD4	KD3	KD2	KD1	KD0	00h
B0h	INTX	R/W	--	--	IX5	IX4	IX3	IX2	IX1	IX0	27h
B1h	INTY	R/W	IY7	IY6	IY5	IY4	IY3	IY2	IY1	IY0	EFh
C0h	TPCR	R/W	AZEN	AZOE	--	SCAN	AS3	AS2	AS1	AS0	00h
C1h	TPSR	R/W	ARDY	ADET	1	1	AF1	AF0	--	--	0Fh
C8h	TPXR	RO	TPX9	TPX8	TPX7	TPX6	TPX5	TPX4	TPX3	TPX2	00h
C9h	TPYR	RO	TPY9	TPY8	TPY7	TPY6	TPY5	TPY4	TPY3	TPY2	00h
CAh	TPZR	RO	TPX1	TPX0	--	--	TPY1	TPY0	--	--	00h
D0h	LCCR	R/W	DZEN	--	--	DAC4	DAC3	DAC2	DAC1	DAC0	8Fh
E0h	PNTR	R/W	FD7	FD6	FD5	FD4	FD3	FD2	FD1	FD0	00h
F0h	FNCR	R/W	TNS	BNK	RM1	RM0	FDA	ASC	ABS1	ABS0	92h
F1h	FVHT	R/W	FH1	FH0	FV1	FV0	1	1	1	1	0Fh

REGISTER DESCRIPTION

REG [00h] Whole Chip LCD Controller Register (**WLCR**)

Bit	Description	Text/Graph	Default	Access
7-6	**Power Mode** 1 1 : Normal Mode. All of the functions of RA8803/8822 are available in this mode. 0 0 : Off Mode. When RA8803/8822 is in off mode, all of functions enter power-off mode, except the wake-up trigger block. If wake-up event occurred, RA8803/8822 would wake-up and return to Normal mode.	--	3h	R/W
5	**Software Reset:** 1 : Reset all registers except flushing RAM 0 : Normal Operation	--	0h	R/W
4	Reserved.	--	0h	R/W
3	**Display Mode Selection** 1 : Character Mode. The written data will be treated as a GB/BIG/ASCII code. 0 : Graphical Mode. The written data will be treated as a bit-map pattern.	--	1h	R/W
2	**Set Display On/Off Selection** The bit is used to control LCD Driver Interface signals -- DISP_OFF. 1 : DISP_OFF pin output high(Display On). 0 : DISP_OFF pin output low(Display Off).	Text/Graph	0h	R/W
1	**Blink Mode Selection** 1 : Blink Full Screen. The blink time is set by register BTMR. 0 : Normal Display.	Text/Graph	0h	R/W
0	**Inverse Mode Selection** 1 : Normal Display 0 : Inverse Full Screen. It will cause the display inversed.	Text/Graph	1h	R/W

REG [01h] Misc. Register (**MISC**)

Bit	Description	Default	Access
7	Reserved.	1h	R/W
6	**Clock Output (Pin CLK_OUT) Control** 1 : Enable 0 : Disable	1h	R/W
5	Reserved.	1h	R/W
4	**Interrupt (INT) and Busy Polarity** 1 : Set Active High	1h	R/W

	0 : Set Active Low		
3-2	Reserved.	0h	R/W
1-0	**Clock Speed Selection** 0 0 : 3MHz 0 1 : 4MHz 1 0 : 8MHz 1 1 : 12MHz	0h	R/W

REG [02h] Advance Power Setup Register (**APSR**)

Bit	Description	Default	Access
7-6	Reserved	0h	R/W
5-4	**ROM/RAM Reading Speed** 0 0 : Speed0 (30ns@Vdd=3.3V) 0 1 : Speed1 (60ns@Vdd=3.3V) 1 0 : Speed2 (90ns@Vdd=3.3V) 1 1 : Speed3 (120ns@Vdd=3.3V)	1h	R/W
3	**Font ROM Readable for MPU** 1 : Enable 0 : Disable	0h	R/W
2	Reserved	0h	R/W
1	Scrolling Reset for Start 0 : Disable 1 : Enable	0h	R/W
0	Reserved	0h	R/W

REG [03h] Advance Display Setup Register (**ADSR**)

Bit	Description	Default	Access
7-4	Reserved	8h	R/W
3	**Set Display RAM Order (Byte)** 1 : Inverse Data of Byte 0 : Normal Mode	0h	R/W
2	**Common Auto Scrolling** 1 : Enable 0 : Disable	0h	R/W
1	**Segment Auto Scrolling** 1 : Enable 0 : Disable	0h	R/W
0	**Common or Segment Scrolling Selection** 1 : Segment Scrolling 0 : Common Scrolling In Extension Mode(REG[12h]： bit[6:4] = “110” or ”111”), this bit must be high.	0h	R/W

REG [10h] Whole Chip Cursor Control Register (**WCCR**)

Bit	Description	Text/Graph	Default	Access
7	**Auto Increase Cursor Position in Reading DDRAM Operation.** 1 : Enable (Auto Increase) 0 : Disable	Text/Graph	0h	R/W
6	**Chinese/English Character Alignment** 1 : Enable 0 : Disable The bit only valid in character mode, that can align full-size and half-size mixed font.	Text	1h	R/W
5	**Store Current Data to DDRAM** 1 : Store Current Data to DDRAM Directly 0 : Store Current Data to DDRAM Inversely	Text/Graph	1h	R/W
4	**Bold Font** (Character Mode Only) 1 : Bold Font 0 : Normal Font	Text	0h	R/W
3	**Auto Increase Cursor Position in Writing DDRAM Operation.** 1 : Enable (Auto Increase) 0 : Disable	Text/Graph	1h	R/W
2	**Cursor Display** 1 : Set Cursor Display On 0 : Set Cursor Display Off	Text/Graph	1h	R/W
1	**Cursor Blinking** 1 : Blink Cursor. The blink time is determined by BTMR. 0 : Normal	Text/Graph	1h	R/W
0	**Cursor Width** 1 : Cursor width is auto adjust by input data. When half size font, the width is one bit(8 Pixel). When full size font, the width is two bit(16 Pixel). 0 : Cursor is fixed at one byte width(8 Pixel).	Text	1h	R/W

REG [11h] Distance of Words or Lines Register (**DWLR**)

Bit	Description	Default	Access
7-4	**Set Cursor Height**	2h	R/W
3-0	**Set Line Distance**	2h	R/W

REG [12h] Memory Access Mode Register (**MAMR**)

Bit	Description	Default	Access
7	**In Graphic Mode, Cursor Auto Shifting Direction** 1 : Horizontal moving first then Vertical. 0 : Vertical moving first then Horizontal.	1h	R/W
6-4	**Display Layer Selection** 0 0 1 : Only Show Page1 0 1 0 : Only Show Page2 0 1 1 : Show Two Layer Mode. The display rule depends on Bit3 and Bit2 as following. 0 0 0 : Gray Mode. In this mode, each pixel gray of LCD depends on the value of Page1 & Page2. Page1 Page2 Gray --- 0 0 Level1 1 0 Level2 0 1 Level3 1 1 Level4 1 1 0 : Extension Mode(1), the panel will show both Page1 and Page2. The RA8803 is available for 640x240 dots panel, and RA8822 for 480x160 dots panel. 1 1 1 : Extension Mode(2), the panel will show both Page1 and Page2. The RA8803 is available for 320x480 dots panel, and RA8822 for 240x320 dots panel.	1h	R/W
3-2	**Two Layer Mode Selection** 0 0 : Page1 RAM “OR” Page2 RAM 0 1 : Page1 RAM “XOR” Page2 RAM 1 0 : Page1 RAM “NOR” Page2 RAM 1 1 : Page1 RAM “AND” Page2 RAM Please refer to Figure 7-10 for more explanation.	0h	R/W
1-0	**MPU Read/Write Layer Selection** 0 0 : Access Page0 (512B SRAM) Display Data RAM. 0 1 : Access Page1 (9.6KB SRAM) Display Data RAM. 1 0 : Access Page2 (9.6KB SRAM) Display Data RAM. 1 1 : Access Page1 and Page2 Display Data RAM at the same time. The Page0 are used for create some temporary characters. Please refer to AP Note for more details.	1h	R/W

REG [20h] Active Window Right Register (**AWRR**)

Bit	Description	Default	Access
7-6	Reserved	0h	R
5-0	**Active Window Right Position** → Segment-Right	27h	R/W

Note: REG [20h, 30h, 40h, 50h] are used for the function of change the line and page. Users can use these four Registers to set a block as an active window. When data goes beyond the right boundary of active window (The value is set by REG [20h, 30h, 40h, 50h]), then the cursor will automatically change the line and write in data continuously. It means the cursor will move to the left boundary of active window, which is set by REG [40h]. When the data comes to the bottom line of the right side (set by REG [20h and 30h]), then the cursor will be moved to the first line of the left side automatically and continue to put in data. (set by REG [40h, 50h]).

REG [30h] Active Window Bottom Register (**AWBR**)

Bit	Description	Default	Access
7-0	**Active Window Bottom Position** → Common-Bottom	EFh	R/W

REG [40h] Active Window Left Register (**AWLR**)

Bit	Description	Default	Access
7-6	Reserved	0h	R
5-0	**Active Window Left Position** → Segment-Left	0h	R/W

REG [50h] Active Window Top Register (**AWTR**)

Bit	Description	Default	Access
7-0	**Active Window Top Position** → Common-Top	0h	R/W

REG [21h] Display Window Right Register (**DWRR**)

Bit	Description	Default	Access
7-6	Reserved	0h	R/W
5-0	**Set Display Window Right Position** → Segment-Right **Segment-Right = (Segment Number / 8) – 1** RA8803: If LCD panel resolution is 320*240, the value of the register is: (320 / 8) - 1 = 39 = 27h RA8822: If LCD panel resolution is 240*160, the value of the register is: (240 / 8) - 1 = 29 = 1Dh	27h	R/W

Note: REG[21h, 31h, 41h, 51h] are used to set Display Window Resolution. Users can set the viewing scope of Display RAM. Column Address of RA8803 can be set between 0~27h, and Row Address can be set between 0~EFh. Column Address of RA8822 can be set between 0~1Dh, and Row Address can be set between 0~9Fh. Users can set start and end address first, and then by adding shift function to present the effect of rolling.

REG [31] Display Window Bottom Register (**DWBR**)

Bit	Description	Default	Access
7-0	**Display Window Bottom Position** → Common-Bottom **Common_ Bottom = LCD Common Number –1 + n** RA8803: If LCD panel resolution is 320*240(n=0), the value of the register is: 240 – 1 = 239 = EFh RA8822: If LCD panel resolution is 240*160(n=0), the value of the register is: 160 – 1 = 159 = 9Fh	EFh	R/W

REG [41] Display Window Left Register (**DWLR**)

Bit	Description	Default	Access
7-0	**Display Window Left Position** → Segment-Left Usually set “0h”.	0h	R/W

REG [51] Display Window Top Register (**DWTR**)

Bit	Description	Default	Access
7-0	**Display Window Top Position** → Common-Top Usually set “0h”.	0h	R/W

Note: For some registers setting, please refer the following rule:

1. DWRR≥ AWRR≥ CPXR≥ AWLR≥ DWLR
2. DWBR≥ AWBR≥ CPYR≥ AWTR≥ DWTR

REG [60h] Cursor Position X Register (**CPXR**)

Bit	Description	Default	Access
7-6	Reserved	0h	R
5-0	**Cursor Position of Segment**	0h	R/W

REG [61h] Begin Segment Position Register (**BGSG**)

Bit	Description	Default	Access
7-6	Reserved	0h	R/W
5-0	**Segment Start Position of Scrolling Mode**	0h	R/W

REG [70h] Cursor Position Y Register (**CPYR**)

Bit	Description	Default	Access
7-0	**Cursor Position of Common**	0h	R/W

REG [71h] Scrolling Action Range, Begin Common Register (**BGCM**)

Bit	Description	Default	Access
7-0	**Common Start Position of Scrolling Mode**	0h	R/W

REG [72h] Scrolling Action Range END Common Register (**EDCM**)

Bit	Description	Default	Access
7-0	**Common Ending Position of Scrolling Mode**	EFh	R/W

REG [80h] Blink Time Register (**BTMR**)

Bit	Description	Default	Access
7-0	**Cursor Blink Time** Blinking Time = Bit [7..0] x (1/Frame_Rate) The setup of Frame Rate is depends on the LCD panel.	33h	R/W

REG [81h] Frame Rate Polarity Change at Common_A Register (**FRCA**)

Bit	Description	Default	Access
7-0	**Reserved**	0h	R/W

REG [91h] Frame Rate Polarity Change at Common_B Register (**FRCB**)

Bit	Description	Default	Access
7-0	**Reserved**	0h	R/W

REG [90h] Shift Clock Control Register (**SCCR**)

Bit	Description	Default	Access
7-0	**Shift Clock Cycle** **SCCR = (SCLK x DW) / (Seg x Com x FRM)** SCLK : RA8803/8822 System Clock (Unit : Hz) DW : Bus Width of LCD Driver(Unit : Bit) Seg : Segment Number of LCD Panel(Unit : Pixel) Com : Common Number of LCD Panel (Unit : Pixel) FRM : Frame Rate of LCD Panel(Unit : Hz) **Note:** SYS_DW=0, If LCD Data Bus is 4it then SCCR has to ≥ 4. SYS_DW=1, If LCD Data Bus is 8it then SCCR has to ≥ 2.	4h	R/W

REG [A0h] Interrupt Setup & Status Register (**INTR**)

Bit	Description	Default	Access
7	**Key Scan Interrupt Flag** 1 : Key Scan Detects Key Input 0 : Key Scan doesn't Detect Key Input	0h	R (Read Clear)
6	**Touch Panel Detect** 1 : Touch Panel Touched 0 : Touch Panel Untouched	0h	R (Read Clear)
5	**Cursor Column Status** 1 : The Cursor Column is equal to INTX 0 : The Cursor Column is not equal to INTX	0h	R (Read Clear)
4	**Cursor Row Status** 1 : The Cursor Row is equal to INTY 0 : The Cursor Row is not equal to INTY	0h	R (Read Clear)
3	**Key Scan Interrupt Mask** 1 : Enable Key Scan Interrupt 0 : Disable Key Scan Interrupt	0h	R/W
2	**Touch Panel Interrupt Mask** 1 : Generate interrupt output if touch panel was detected. 0 : Don't generate interrupt output if touch panel was detected.	0h	R/W
1	**Register[B0h] INTX Event Mask** 1 : Enable INTX Interrupt 0 : Disable INTX Interrupt	0h	R/W
0	**Register[B1h] INTY Event Mask** 1 : Enable INTY Interrupt 0 : Disable INTY Interrupt	0h	R/W

REG [A1h] Key Scan Controller Register (**KSCR**)

Bit	Description	Default	Access
7	**Key Scan Enable Bit** 1 : Enable 0 : Disable	0h	R/W
6	**Key Scan Matrix Selection** 1 : 4x4 Matrix 0 : 8x8 Matrix	0h	R/W
5-4	**Key Scan Data Sampling Times** 0 0 : 2h 0 1 : 4h 1 0 : 8h 1 1 : 16h	0h	R/W
3	Reserved	0h	R/W
2-0	**Key Scan Frequency Selection**	0h	R/W

	0 0 0 : 2 x FRM 0 0 1 : 4 x FRM 0 1 0 : 8 x FRM 0 1 1 : 16 x FRM 1 0 0 : 32 x FRM 1 0 1 : 64 x FRM 1 1 0 : 128 x FRM 1 1 1 : 256 x FRM		

REG [A2h] Key Scan Data Register (**KSDR**)

Bit	Description	Default	Access
7-0	**Key Scan KC[7~0] Output**	0h	R

REG [A3h] Key Scan Data Expand Register (**KSER**)

Bit	Description	Default	Access
7-0	**Key Scan KR[7~0] Input**	0h	R

REG [B0h] Interrupt Column Setup Register (**INTX**)

Bit	Description	Default	Access
7-6	Reserved	0h	R
5-0	**Column Address of Interrupt** If Cursor Position X Register (CPXR)=INTX, then an interrupt occurred.	27h	R/W

REG [B1h] Interrupt Row Setup Register (**INTY**)

Bit	Description	Default	Access
7-0	**Row Address of Interrupt** If Cursor Position Y Register (CPYR)=INTY, then an interrupt has occurred.	EFh	R/W

REG [C0h] Touch Panel Control Register (**TPCR**)

Bit	Description	Default	Access
7	**Touch Panel Enable Bit** 1 : Enable 0 : Disable	1h	R/W
6	**Touch Panel Data Output Control** 1 : Enable the Touch Panel Data Output 0 : Disable the Touch Panel Data Output	1h	R/W
5	**Reserved**	0h	R/W
4	**Touch Panel Scan**	1h	R/W

	1 : Disable 0 : Enable		
3-0	**Switch Control of Touch Panel** Bit3: control SW3 ON/OFF(1/0) Bit2: control SW2 ON/OFF(1/0) Bit1: control SW1 ON/OFF(1/0) Bit0: control SW0 ON/OFF(1/0)	Fig. 6-6	R/W

REG [C1h] Touch Panel Status Register (**TPSR**)

Bit	Description	Default	Access
7	**ADC Data Convert State** 1 : Convert Complete 0 : Convert Incomplete	0h	R
6	**Touch Event Indicate** 1 : Touched 0 : Un-touch	0h	R
5	This bit Must be "1" when system initial.	0h	R/W
4	This bit Must be "1" when system initial.	0h	R/W
3-2	**ADC Convert Speed** 0 0 : SCLK/32 0 1 : SCLK/64 1 0 : SCLK/128 1 1 : SCLK/256	2h	R/W
1-0	**Reserved**	2h	R/W

REG [C8h] Touch Panel Segment High Byte Data Register (**TPXR**)

Bit	Description	Default	Access
7-0	**Touch Panel Segment Data Bit[9..2]**	80h	R

REG [C9h] Touch Panel Common High Byte Data Register (**TPYR**)

Bit	Description	Default	Access
7-0	**Touch Panel Common Data Bit[9..2]**	80h	R

REG [CAh] Touch Panel Segment/Common Low Byte Data Register (**TPZR**)

Bit	Description	Default	Access
7-6	**Touch Panel Segment Data Bit[1..0]**	0h	R
5-4	Reserved	0h	--
3-2	**Touch Panel Common Data Bit[1..0]**	0h	R
1-0	Reserved	0h	--

REG [D0h] LCD Contrast Control Register (**LCCR**)

Bit	Description	Default	Access
7	**DAC Function** 1 : Disable 0 : Enable	1h	R/W
6-5	Reserved	0h	--
4-0	**DAC Driving Current** 0 0 0 0 0b (Min. Current) : : : 1 1 1 1 1b (Max. Current)	0Fh	R/W

REG [E0h] Pattern Data Register (**PNTR**)

Bit	Description	Default	Access
7-0	**(1) Data Written to DDRAM** When REG[F0h] bit3 is '1', it will read the data from Register [E0h] and fill the whole DDRAM. After the movement of filling the Active window, REG [F0h] bit3 will become "0". **(2) Display Times of Gray Mode** For Gray Mode(Register MAMR bit[6..4] = 000), These register used to control the display times. If the frame rate is fixed, the number of "1" and "0" are represent the display ratio of 1 and 0. Please see Chapter 7-10 and AP Note 9-23 for more description.	0h	R/W

REG [F0h] Font Control Register (**FNCR**)

Bit	Description	Text/Graph	Default	Access
7	**Font ROM Transfer Circuit** 1 : Enable 0 : Bypass	--	1h	R/W
6	When bit5~4 set as "00" → ROM Mode0, this bit could be used to select the upper or lower part of 256KB ROM. 1 : Select lower part of 256KB ROM 0 : Select upper part of 256KB ROM	--	0h	R/W
5-4	**Select Font ROM Type** 0 0 : Select GB font ROM (256KB, Mode0) 0 1 : Select BIG5 font ROM (512KB, Mode1) 1 0 : Support GB font ROM (512KB, Mode2)	--	1h	R/W
3	**Fill PNTR Data to DDRAM** 1 : Fill Data to DDRAM Enable 0 : No Action	Graph	0h	R/W

	When this bit is "1", RA8803/8822 will automatically read PNTR data, and fill it to DDRAM (Range:[AWLR, AWTR] ~ [AWRR, AWBR]), and then this bit will be cleaned to "0".			
2	**ASCII Code Selection** 1 : All input data will be decoded as ASCII (00~FFh) 0 : The RA8803/8822 will check the first byte data first. If the first byte is 00~9Fh then regarded as ASCII (Half-size). If first byte is A0~FFh then regarded as GB/BIG5 (Full-size).	Text	0h	R/W (Auto Clear)
1-0	**ASCII Blocks Select** 0 0 : Map to ASCII block 0, Latin_1 0 1 : Map to ASCII block 1, Latin_2 1 0 : Map to ASCII block 2, Latin_3 1 1 : Map to ASCII block 3, Latin_4	--	2h	R/W

REG [F1h] Font Size Control Register (**FVHT**)

Bit	Description	Default	Access
7-6	**Set Character Horizon Size** 0 0 : One Time 0 1 : Two Times 1 0 : Three Times 1 1 : Four Times	0h	R/W
5-4	**Set Character Vertical Size** 0 0 : One Time 0 1 : Two Times 1 0 : Three Times 1 1 : Four Times	0h	R/W
3-0	**Reserved**	Fh	R/W

Registers for Display Resolution

Normally the REG[40h], REG[50h], REG[41h] and REG[51h] set to "00h". And the content of REG[20h], REG[30h], REG[21h] and REG[31h] are depend on the resolution of LCD module. The following are reference table of different LCD module.

Registers Setting for LCM Resolution

Segment	Common	REG[20h] AWRR	REG[30h] AWBR	REG[21h] DWRR	REG[31h] DWBR
160	**80**	13h	4Fh	13h	4Fh
160	**128**	13h	7Fh	13h	8Fh (Note)
160	**160**	13h	9Fh	13h	9Fh
240	**64**	1Dh	3Fh	1Dh	3Fh
240	**128**	1Dh	7Fh	1Dh	8Fh (Note)
240	**160**	1Dh	9Fh	1Dh	9Fh
320	**240**	27h	EFh	27h	EFh

Note : n = 10h，DWBR = (LCD Common Number –1) + n = 128-1+10h = 8Fh。

A.C. CHARACTERISTICS

1. For 8080 series :

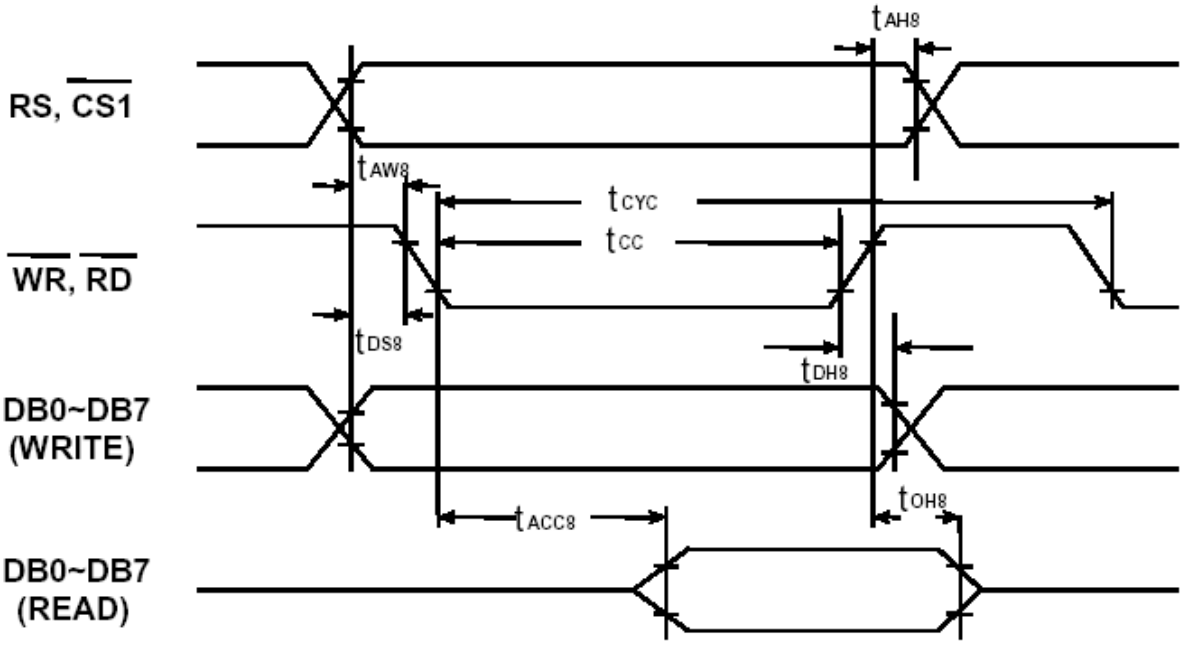
Signal	Symbol	Parameter	Rating		Unit	Condition
			Min	Max		
RS, CS1#	t_{AH8}	Address hold time	10	--	ns	System Clock: 8MHz Voltage: 3.3V
	t_{Aw8}	Address setup time	63	--	ns	
WR#, RD#	t_{CYC}	System cycle time	800	--	ns	
	t_{CC}	Strobe pulse width	400	--	ns	
DB0 to DB7	t_{DS8}	Data setup time	63	--	ns	
	t_{DH8}	Data hold time	10	--	ns	
	t_{ACC8}	RD access time	--	330	ns	
	t_{OH8}	Output disable time	10	--	ns	

2. For 6800 series :

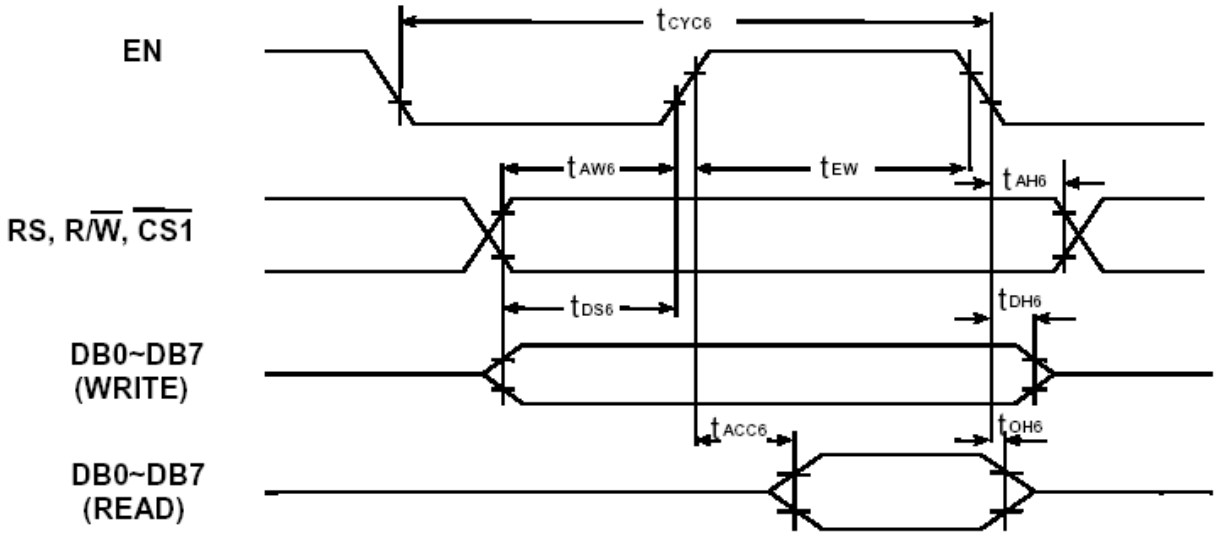
Signal	Symbol	Parameter	Rating		Unit	Condition
			Min	Max		
A0, R/W#, CS1#	t_{AH6}	Address hold time	10	--	ns	System Clock: 8MHz Voltage: 3.3V
	t_{Aw6}	Address setup time	63	--	ns	
	t_{CYC6}	System cycle time	800	--	ns	
DB0 to DB7	t_{DS6}	Data setup time	63	--	ns	
	t_{DH6}	Data hold time	10	--	ns	
	t_{ACC6}	Access time	--	330	ns	
	t_{OH6}	Output disable time	10	--	ns	
EN	t_{EW}	Enable pulse width	400	--	ns	

TIMING DIAGRAMS

1. For 8080 series :



2. For 6800 series :

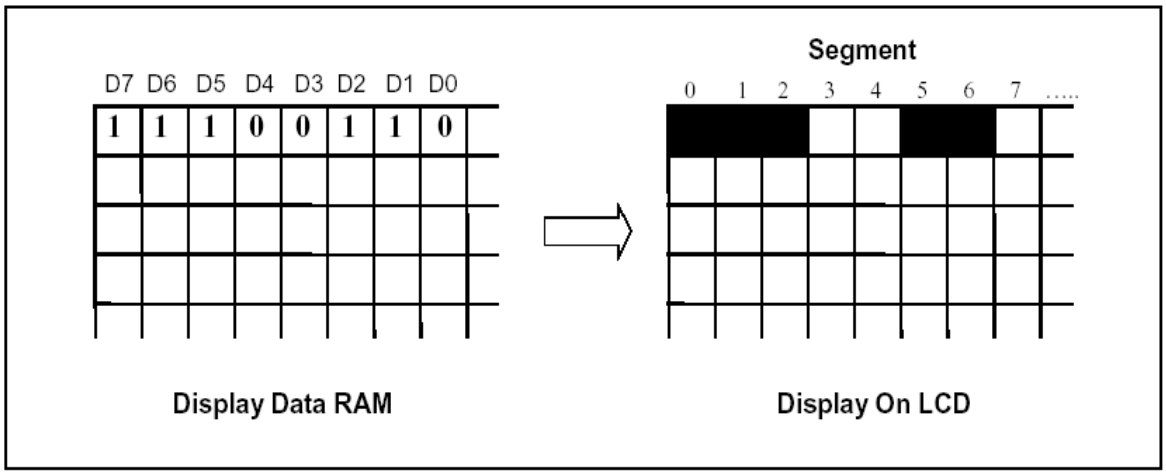


DATA ACCESS WITH MCU

No.	RS	6800	8080		DB0-DB7	Function
		R/W#	RD#	WR#		
①	1	1	0	1	xxh	Read Display Data
②	1	0	1	0	High Byte -->Low Byte	Write Display Data (Character Mode – Chinese): Execute Step ② twice. At first, write the High Byte of Chinese Code, then write Low Byte.
③	1	0	1	0	xxh	Write Display Data (Character Mode – English, ASCII)
④	1	0	1	0	xxh	Write Display Data (Graphic Mode)
⑤	0	0	1	0	Address	Read Data(Status) from Register: Step ⑤ → Step ⑥
⑥	0	1	0	1	Status	
⑦	0	0	1	0	Address	Write Command to Register: Step ⑦ → Step ⑧
⑧	0	0	1	0	Command	

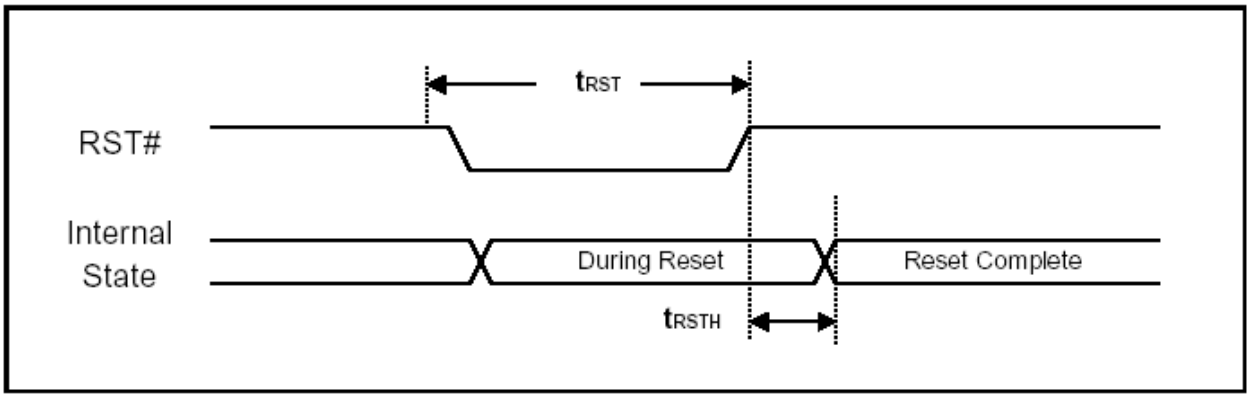
DISPLAY DATA RAM

The RA8803 embedded two 9.6Kbyte display RAM for two layers display. It supports the maximum resolution of LCD panel is 320Column x 240Row. RA8822 embedded two 4.8Kbyte display RAM and support 240Column x 160Row for maximum resolution. The RA8803/8822 support both text and graphics mode. The user could switch both two modes at any time.



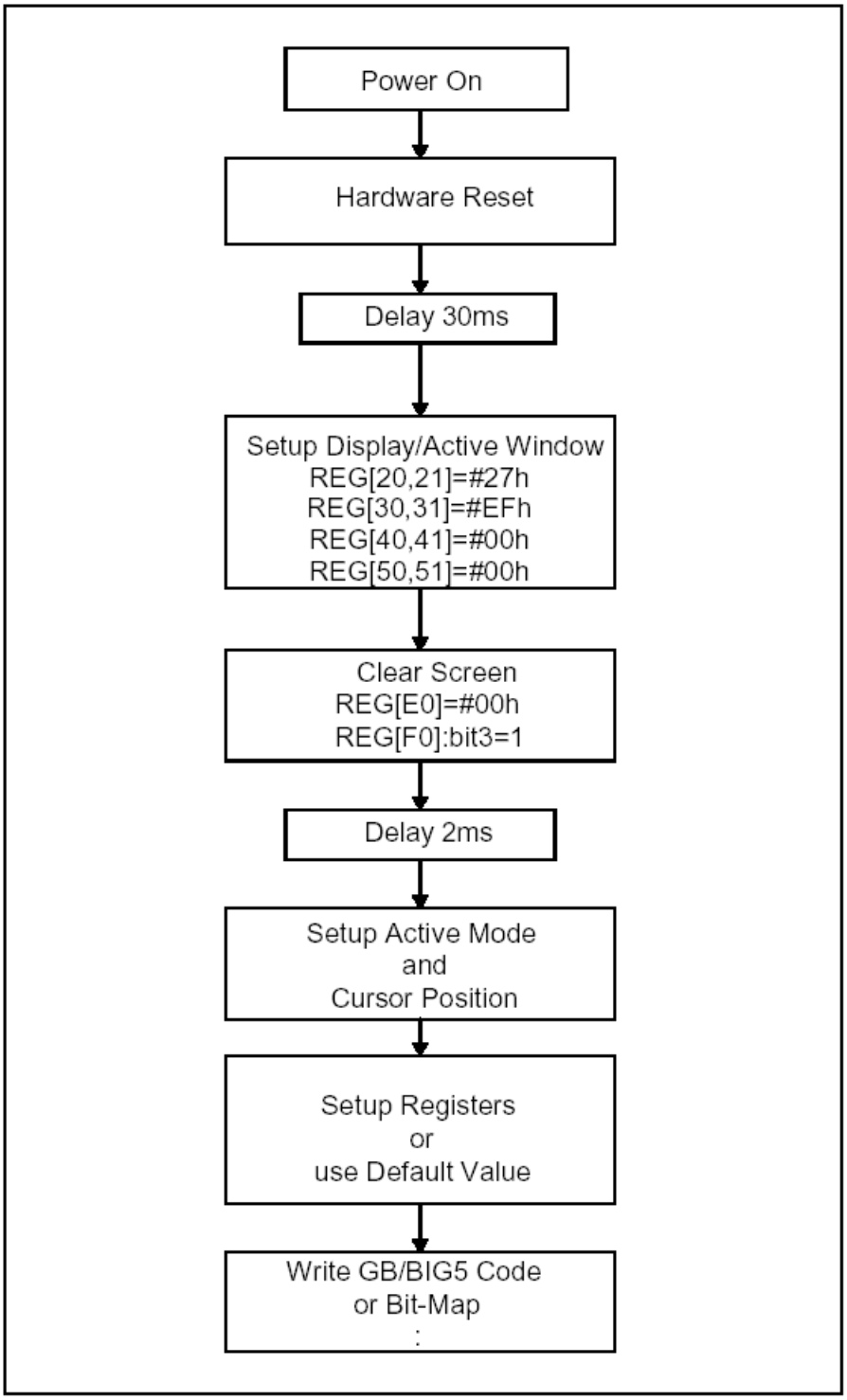
POWER ON/RESET PROCESS

Reset timing of RA8803/8822. For example, if the panel resolution is 320x240 pixel, then t_{RST} must over 250ms and t_{RSTH} must over 50ms. The RA8803/8822 Reset need enough time to complete the reset procedure.



Reset timing

The following figure is a procedure of RA8803/8822 power On/Reset.



RA8803/8822 Power On/Reset Process

ELECTRO-OPTICAL CHARACTERISTICS

MEASURING CONDITION: POWER SUPPLY = V_{OP} / 64 Hz
TEMPERATURE = 23 ± 5 °C
RELATIVE HUMIDITY = 60 ± 20 %

ITEM	SYMBOL	UNIT	TYP. STN
RESPONSE TIME	Ton	ms	370
	Toff	ms	470
CONTRAST RATIO	Cr	-	7
VIEWING ANGLE (Cr ≥ 2)	$V_{3:00}$	°	40
	$V_{6:00}$	°	50
	$V_{9:00}$	°	40
	$V_{12:00}$	°	30

THE ELECTRO-OPTICAL CHARACTERISTICS ARE MEASURED VALUE BUT NOT GUARANTEED ONES.

RELIABILITY OF LCD MODULE

ITEM	TEST CONDITION FOR NORMAL TEMPERATURE	TEST CONDITION FOR WIDE TEMPERATURE	TIME
High temperature operating	50°C	70°C	240 hours
Low temperature operating	0°C	-20°C	240 hours
High temperature storage	60°C	80°C	240 hours
Low temperature storage	-10°C	-30°C	240 hours
Temperature-humidity storage	40°C 90% R.H.	60°C 90% R.H.	96 hours
Temperature cycling	-10°C to 60°C 30 Min Dwell	-30°C to 80°C 30 Min Dwell	5 cycle
Vibration Test at LCM Level	Freq 10-55 Hz Sweep rate: 10-55-10 at 1 min Sweep mode Linear Displacement: 2 mm p-p 1 Hour each for X, Y, Z	Freq 10-55 Hz Sweep rate: 10-55-10 at 1 min Sweep mode Linear Displacement: 2 mm p-p 1 Hour each for X, Y, Z	—

SAMPLING METHOD

SAMPLING PLAN: MIL-STD 105E

CLASS OF AQL: LEVEL II/ SINGLE SAMPLING
MAJOR-0.65% MINOR – 1.5%

DEFECT	CRITERIA	TYPE	FIGURE
SHORT CIRCUIT	-	MAJOR	-
MISSING SEGMENT	-	MAJOR	-
UNEVEN / POOR CONTRAST	-	MAJOR	-
CROSS TALK	-	MAJOR	-
PIN HOLE	MAX(a,b) ≤ 1 / 4 W	MINOR	1
EXCESS SEGMENT	MAX(c,d) ≤ 1 / 4 T	MINOR	1
BUBBLES	d* ≥ 0.3 QTY=0	MINOR	2
SPOTS	d ≤ 0.3 N.A.** 0.3<d≤0.4 QTY≤2 0.4<d QTY=0	MINOR	2
LINE SCRATCHES	x≥0.7 y≥0.05 QTY=0	MINOR	3
BLACK LINE	x≥0.7 y≥0.05 QTY=0	MINOR	3

* d = MAX (d_1,d_2) ** N. A . = NOT APPLICABLE DEFECT TABLE : C

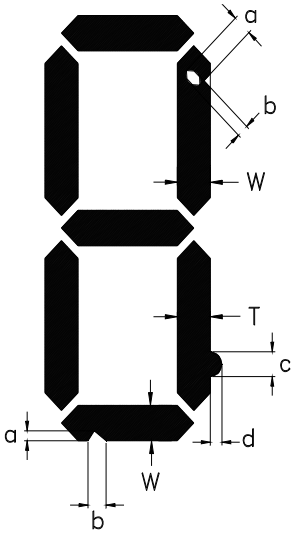
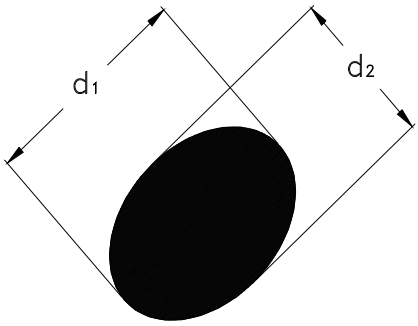
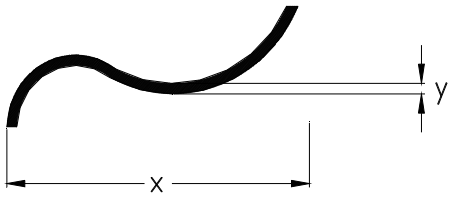


fig . 1



POLARIZER BUBBLES / SPOTS
fig . 2



LINE SCRATCHES / BLACK LINE
fig . 3

QUALITY STANDARD (CONT .)

DEFECT		CRITERIA	TYPE	FIGURE
CHIPS	CONTACT EDGE	e≤1/2T f≤1/3W g≤4.0	MINOR	4
	BOTTOM GLASS	p≤1.5 q≤3.5 r≤1/2T		4
	CORNER	a≤2.0 b≤W		4
	TOP GLASS	a≤3.5 b≤1/3T c≤1/2W		5
GLASS PROTRUSION		a ≤ 1/4 W	MINOR	6
RAINBOW		-	MINOR	-

UNLESS STATE OTHERWISE , ALL UNIT ARE IN MILLIMETER . DEFECT TABLE : C

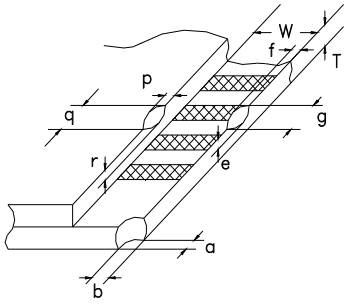


fig . 4

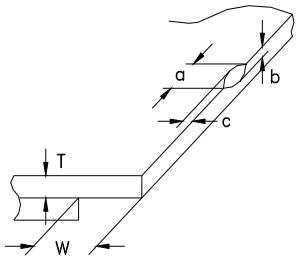


fig . 5

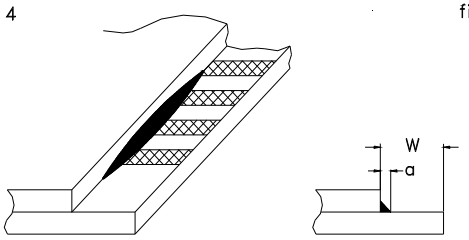


fig . 6

QUALITY STANDARD OF LCD MODULE

1.0	**Sampling Method**		
	Sampling Plan : MIL STD 105 E Class of AQL : Level II/Single Sampling Critical : 0.25% Major 0.65% Minor 1.5%		
2.0	**Defect Group**	**Failure Category**	**Failure Reasons**
	Critical Defect 0.25%(AQL)	Malfunction	Open Short Burnt or dead component Missing part/improper part P.C.B. Broken
	Major Defect 0.65%(AQL)	Poor Insulation	Potential short High current Component damage or scratched or Lying too close improper coating
		Poor Conduction	Damage joint Wrong polarity Wrong spec. part Uneven/intermittent contact Loose part Copper peeling Rust or corrosion or dirt‘s
	Minor Defect 1.5%(AQL)	Cosmetic Defect	Minor scratch Flux residue Thin solder Poor plating Poor marking Crack solder Poor bending Poor packing Wrong size

HANDLING PRECAUTIONS

(1) CAUTION OF LCD HANDLING & CLEANING

The polarizing plate on the surface of the panel is made from organic substances. Be very careful for chemicals not to touch the plate or it leads the polarizing plate to deteriorate.

If the use of a chemical is unavoidable, wipe the panel lightly with soft materials, such as gauze and absorbent cotton, soaked in a solvent.

*Usable solvent: Alcohol (ethanol, IPA and the like)
*Appropriate solvent: Ketones, ethyl alcohol

Avoid wiping with a dry cloth, since it could damage the surface of the polarizing plate and others.
Do not expose to direct sunlight or fluorescent light for a long time

(2) CAUTION AGAINST STATIC CHARGE

The LCD modules use CMOS LSI drivers, so customers are recommended that any unused input terminal would be connected to V_{DD} or V_{SS} , do not input any signals before power is turned on, and ground your body, work/assembly areas, assembly equipment to protect against static electricity.

(3) ESD PRECAUTION

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is recommended to take normal precautions appropriate to handling LCM module. For example: product surface grounding.

Always take ESD precaution when handling the *LCD Module*. Components are exposed for direct finger touches and can be damaged unless ESD precaution is taken.

(4) PACKAGING

Avoid intense shock and falls from a height and do not operate or store them exposed to direct sunshine or high temperature/humidity for long periods.

(5) CAUTION FOR OPERATION

The viewing angle can be adjusted by varying the LCD driving voltage VO.

Driving voltage should be kept within specified range, excess voltage shortens display life.

Response time increases with decrease in temperature.

Display may turn black or dark Blue at temperature above its operational range; this is however not destructive and the display will return to normal once the temperature falls back to range.

Mechanical disturbance during operation (such as pressing on the viewing area) may cause the segments to appear “fractured”. They will recover once the display is turned off.

Condensation at terminals will cause malfunction and possible electrochemical reaction. Relative humidity of the environment should therefore be kept below 60%.

(6) SAFETY

Liquid crystal may leak out of a damaged LCD, it is recommended to wash off the liquid crystal by using solvents such as acetone or ethanol and should be burned up later.

If any liquid leak out of a damaged glass cell comes in contact with your hands, wash it off with soap and water immediately.

WARRANTY

CLOVER will replace or repair any of her LCD module in accordance with her LCD specification for a period of one year from date of shipment. The warranty liability of Clover is limited to repair and/or replacement. Clover will not be responsible for any subsequent or consequential event.