# FM25Q64

## 64M-BIT

## Serial Flash Memory with 4KB Sectors, Dual and Quad I/O SPI

## Documents title

64M bit Serial Flash Memory with 4KB Sectors, Dual and Quad I/O SPI

## Revision History

| Revision No. | History | Draft date | Remark |
|---|---|---|---|
| 0.0 | Initial Draft | Jul.2010 | preliminary |
| 0.1 | Write Status Register (01h)<br>previous bits => cleared to 0 Change<br>Read instructions tSHSL20ns => 10ns Change | Aug.18.2010 | preliminary |

# Table of Contents

## 1. GENERAL DESCRIPTION

The FM25Q64 Serial Flash memory provides a storage solution for systems with limited space, pins and power. The 25Q series offers flexibility and performance well beyond ordinary Serial Flash devices. They are ideal for code shadowing to RAM, executing code directly from Dual/Quad SPI (XIP) and storing voice, text and data. The devices operate on a single 2.7V to 3.6V power supply with current consumption as low as 5mA active and 1µA for power-down. All devices offered in space-saving packages.

The FM25Q64 array is organized into 32.786 programmable pages of 256-bytes each. Up to 256 bytes can be programmed at a time using the Page Program instructions. Pages can be erased in groups of 16 (4KB sector erase) groups of 128 (32KB block erase), groups of 256 (64KB block erase) or the entire chip (chip erase). The FM25Q64 has 2,048 erasable sectors and 128 erasable blocks respectively. The small 4KB sectors allow for greater flexibility in applications that require data and parameter storage.

The FM25Q64 supports the standard Serial peripheral Interface (SPI), and a high performance Dual output as well as Dual I/O SPI using pins: Serial Clock, Chip Select, Serial Data I/O0(DI), Serial Data I/O1(DO). SPI clock frequencies of up to 104MHz are supported allowing equivalent clock rates of 208MHz for Dual Output and 416Mhz for Quad Output when using the Fast Read Dual/Quad Output instructions. These transfer rates are comparable to those of 8 and 16-bit Parallel Flash memories.

A Hold pin, Write protect pin and programmable write protection, with top or bottom array control, provide further control flexibility. Additionally, the device supports JEDEC standard manufacturer and device identification with a 4K-bit Secured OTP.

## 2. FEATURES

- **SpiFlash Memory**
  - FM25Q64: 64M-bit / 8M–byte
  - 256-bytes per programmable page
  - 4K-bit secured OTP
- **Standard, Dual or Quad SPI**
  - standard SPI: CLK, /CS, DI, DO, /WP, /Hold
  - Dual SPI: CLK, /CS, $IO_0$, $IO_1$, /WP, /Hold
  - Quad SPI: CLK, /CS, $IO_0$, $IO_1$, $IO_2$, $IO_3$
- **Highest Performance Serial Flash**
  - Up to 7X that of ordinary Serial Flash
  - 104MHz clock operation
  - 208MHz equivalent Dual SPI
  - 416MHz equivalent Quad SPI
  - 50MB/S continuous data transfer rate
  - 31MB/S random access (32-byte fetch)
  - Comparable to X16 Parallel Flash
- **Package Material**
  - Fidelix all product Green package
    Lead-free
    RoHS Compliant
    Halogen-free
- **Advanced Security Features**
  - Software and Hardware Write-protect
  - Top or Bottom, Sector or Block selection
  - Lock-Down and OTP protection
- **Flexible Architecture with 4KB sectors**
  - Uniform Sector Erase (4K-byte)
  - Uniform Block Erase (32K and 64K-bytes)
  - program one to 256 bytes
  - Up to 100,000 erase/write cycles
  - 20-years data retention
  - Erase/Program Suspend & Resume
- **Low Power, wide Temperature Range**
  - Single 2.7 to 3.6V supply
  - 5mA active current, <1µA Power-down (typ.)
  - -40℃ to +85℃ operating range
- **Space Efficient Packaging**
  - 8-pin SOIC 208mil
  - 16-pin SOIC 300-mil
  - 8-pin DIP 300mil
  - 8-pad WSON 6x5-mm

## 3. PIN CONFIGURATION SOIC 208-MIL

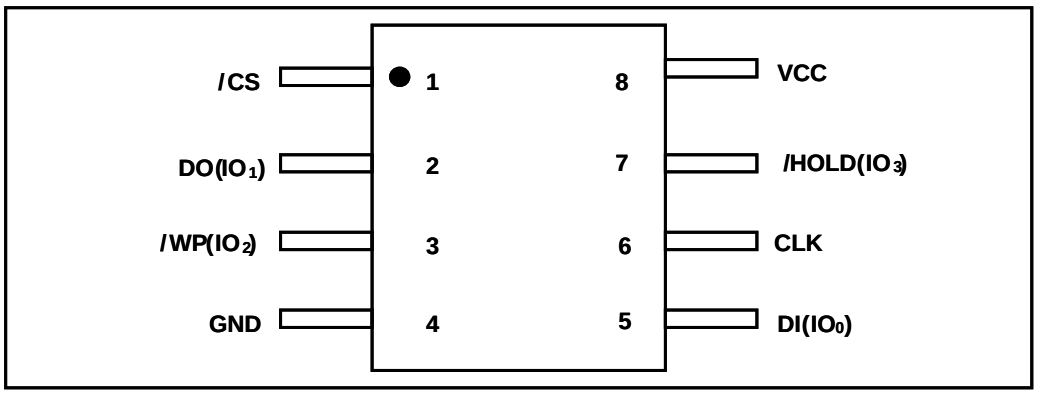



Figure 1a. pin Assignments, 8-pin SOIC 208-mil

## 4. PAD CONFIGURATION WSON 6X5-MM

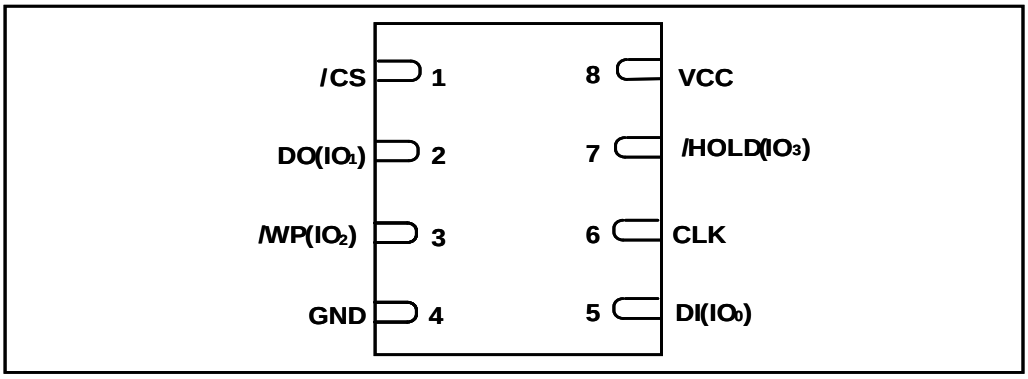



Figure 1b. Pad Assignments, 8-pad WSON

## 5. PIN CONFIGURATION 8-Pin PDIP 300-Mil

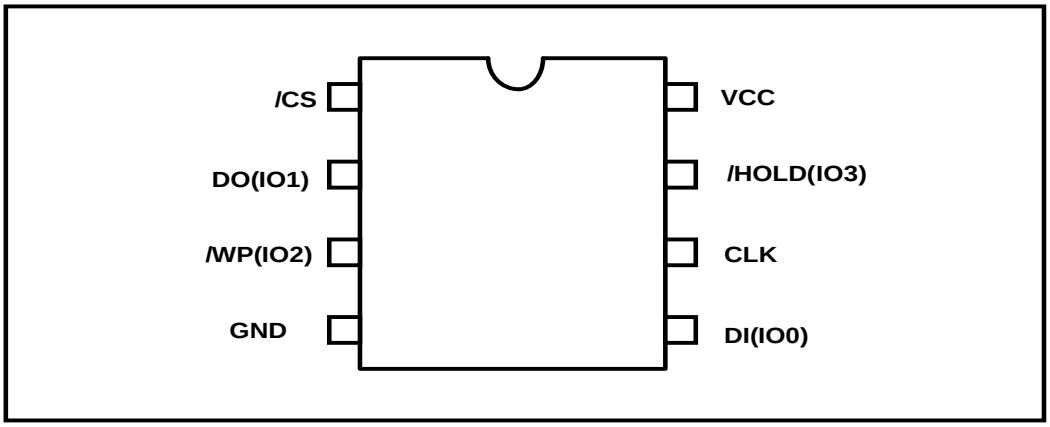



Figure 1c. Assignments, 8-pin PDIP 300-mil

## 6. PIN DESCRIPTION SOIC 208-MIL, PDIP 300MIL AND WSON 6X5MM

| PIN NO. | PIN NAME | I/O | FUCTION |
|---|---|---|---|
| 1 | /CS | I | Chip Select Input |
| 2 | DO(IO1) | I/O | Data Output (Data Input Output 1)*1 |
| 3 | /WP(IO2) | I/O | Write Protect Input (Data Input output) *2 |
| 4 | GND | | Ground |
| 5 | DI(IO0) | I/O | Data Input (Data Input Output 0)*1 |
| 6 | CLK | I | Serial Clock Input |
| 7 | /HOLD(IO3) | I/O | Hold Input (Data Input output 3) *2 |
| 8 | VCC | | Power Supply |

*1 IO0 and IO1 are used for Dual and Quad instructions
*2 IO0－IO3 are used for Quad instructions

## 7. PIN CONFIGURATION SOIC 300-MIL

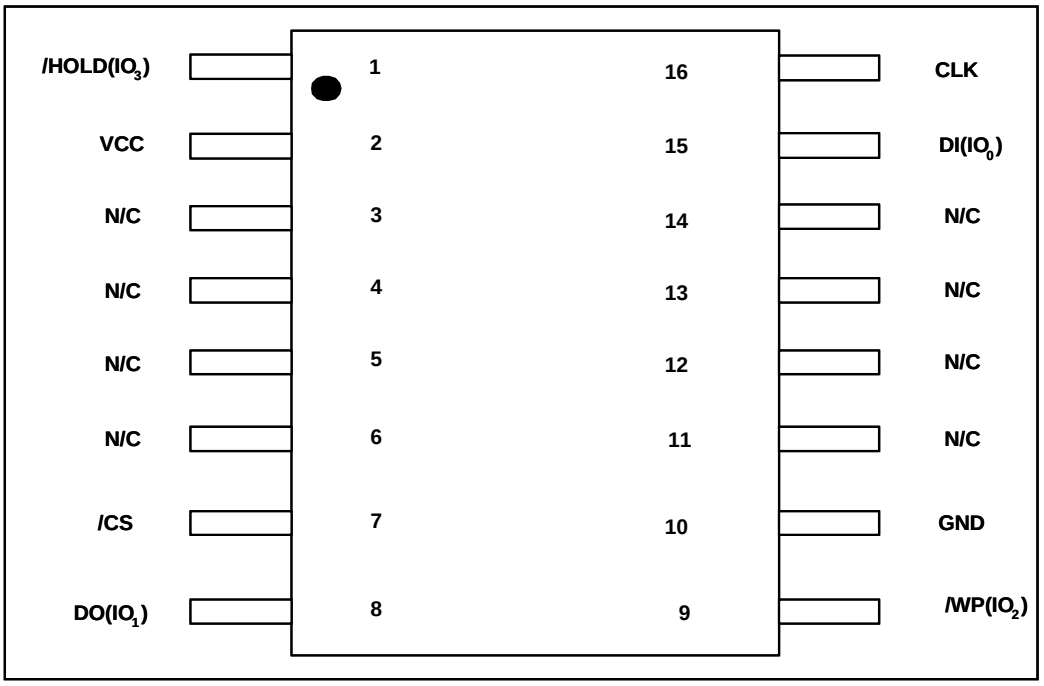



Figure 1d. Pin Assignments, 16-pin SOIC 300-mil

## 8. PIN DESCRIPTION SOIC 300-MIL

| PAD NO. | PAD NAME | I/O | FUCTION |
|---|---|---|---|
| 1 | /HOLD(IO3) | I/O | Hold Input(Data Input Output 3)* 2 |
| 2 | VCC | | Power Supply |
| 3 | N/C | | No Connect |
| 4 | N/C | | No Connect |
| 5 | N/C | | No Connect |
| 6 | N/C | | No Connect |
| 7 | /CS | I | Chip Select Input |
| 8 | DO(IO1) | I/O | Data output (Data Input Output 1)* 1 |
| 9 | /WP(IO2) | I/O | Write Protection Input (Data Input Output 2)* 2 |
| 10 | GND | | Ground |
| 11 | N/C | | No Connect |
| 12 | N/C | | No Connect |
| 13 | N/C | | No Connect |
| 14 | N/C | | No Connect |
| 15 | DI(IO0) | I/O | Data Input (Data Input Output 0)* 1 |
| 16 | CLK | I | Serial Clock Input |

*1 IO0 and IO1 are used for Dual and Quad instructions
*2 IO0_IO3 are used for Quad instructions

## 8.1 Package Types

8-pin plastic 208-mil width SOIC, 6x5-mm WSON, 8-pin PDIP and 16-pin plastic 300-mil width SOIC as shown in figure 1a, 1b,1c and 1d respectively.
Package diagrams and dimensions are illustrated at the end of this datasheet.

## 8.2 Chip Select (/CS)

The SPI Chip Select (/CS) pin enables and disables device operation. When /CS is high the device is deselected and the Serial Data Output (DO, or IO0, IO1, IO2, IO3) pins are at high impedance. When deselected, the device power consumption will be at standby levels unless an internal erase, program or write status register cycle is in progress. When /CS is brought low the device will be selected, power consumption will increase to active levels and instructions can be written to and read data from the device. After power-up, /CS must transition from high to low before a new instruction will be accepted. The /CS input must track the VCC supply level at power-up (see "Write Protection" and figure 30). If needed a pull-up resister on /CS can be used to accomplish this.

## 8.3 Serial Data Input, Output and IOs (DI, DO and IO0, IO1, IO2, IO3)

The FM25Q64 supports standard SPI, Dual SPI and Quad SPI operation. Standard SPI instructions use the unidirectional DI (input) pin to serially write instructions, addresses or data to the device on the rising edge of the Serial Clock (CLK) input pin. Standard SPI also uses the unidirectional DO (output) to read data or status from the device on the falling edge of CLK.

Dual and Quad SPI instructions use the bidirectional IO pins to serially write instructions, addresses or data to the device on the rising edge of CLK and read data or status from the device on the falling edge of CLK. Quad SPI instructions require the non-volatile Quad Enable bit (QE) in Status Register-2 to be set. When QE=1 the /WP pin becomes IO2 and /HOLD pin becomes IO3.

## 8.4 Write Protect (/WP)

The Write Protect (/WP) pin can be used to prevent the Status Register from being written. Used in conjunction with the Status Register's Block Protect (SEC. TB. BP2, Bp1 and BP0) bits and Status Register Protect (SRP) bits, a portion or the entire memory array can be hardware protected. The /WP pin is active low. When the QE bit of Status Register-2 is set for Quad I/O, the /WP pin (Hardware Write Protect) function is not available since this pin is used for IO2. See figure 1a, 1b, 1c and 1d for the pin configuration of Quad I/O operation.

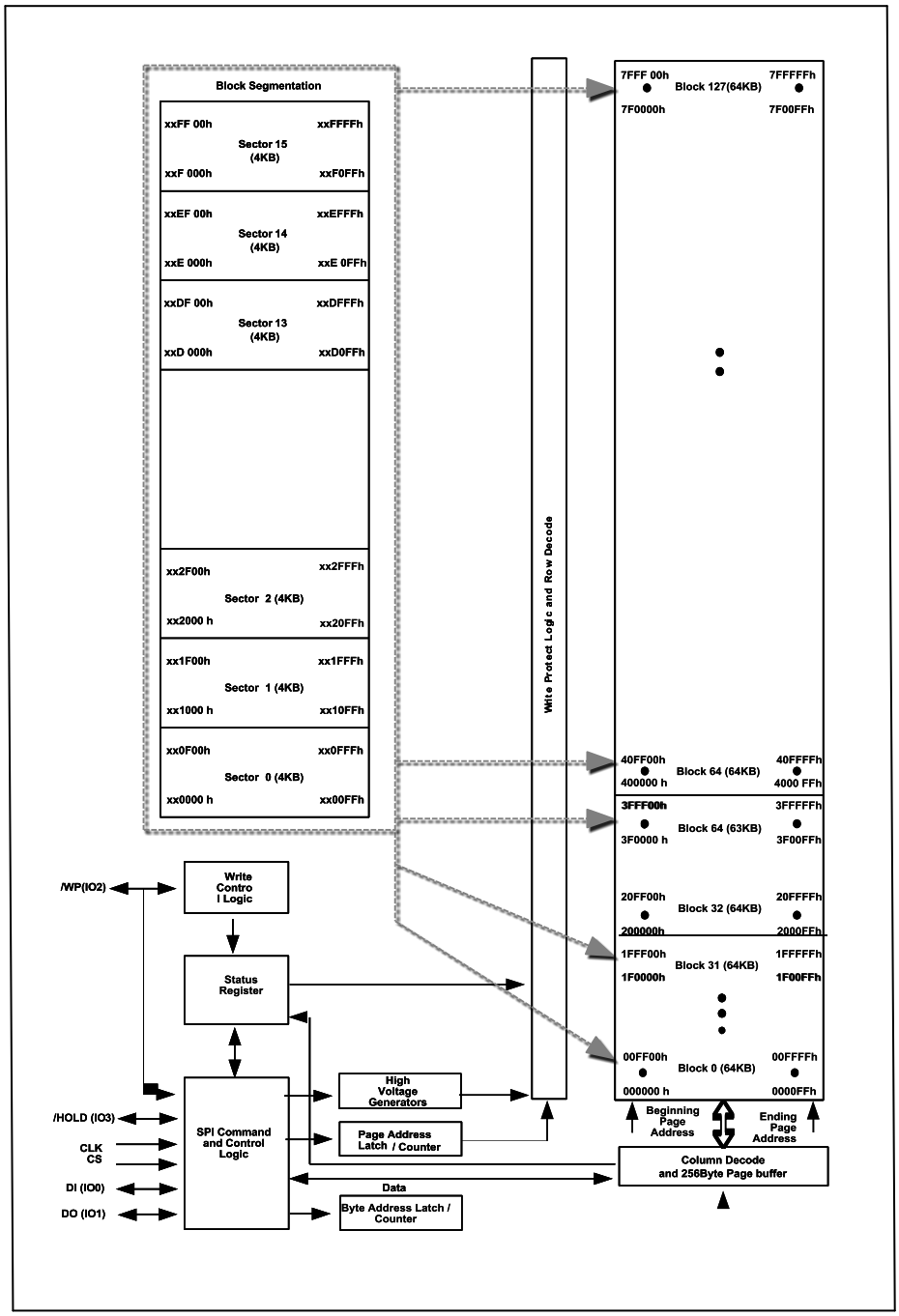
## 8.5 HOLD (/HOLD)

The /HOLD pin allows the device to be paused while it is actively selected. When /HOLD is brought low, while /CS is low, the DO pin will be at high impedance and signals on the DI and CLK pins will be ignored (don't care). When /HOLD is brought high, device operation can resume. The /HOLD function cab be useful when multiple devices are sharing the same SPI signals. The /HOLD pin is active low. When the QE bit of Status Register-2 is set Quad I/O, the /HOLD pin function is not available since this pin used for IO3. See figure 1a, 1b, 1c and 1d for the pin configuration of Quad I/O operation.

## 8.6 Serial Clock (CLK)

The SPI Serial Clock Input (CLK) pin provides the timing for serial input and output operations. ("See SPI Operations")

# 9. BLOCK DIAGRAM



# 10. FUNCTIONAL DESCRIPTION

## 10.1 SPI OPERATIONS

### 10.1.1 Standard SPI Instructions

The FM25Q64 is accessed through an SPI compatible bus consisting of four signals: Serial Clock (CLK). Chip Select (/CS), Serial Data Input (DI) and Serial Data Output (DO). Standard SPI instructions use the DI input pin to serially write instructions, addresses or data to the device on the rising edge of CLK. The DO output pin is used to read data or status from the device on the falling edge of CLK.

SPI bus operation Modes 0 (0, 0) and 3 (1, 1) are supported. The primary difference between Mode 0 and Mode 3 concerns the normal state of the CLK signal when the SPI bus master is in standby and data is not being transferred to the Serial Flash. For Mode 0 the CLK signal is normally low on the falling and rising edges of /CS. For Mode 3 the CLK signal is normally high on the falling and rising edges of /CS.

### 10.1.2 Dual SPI Instructions

The FM25Q64 supports Dual SPI operation when using the “Fast Read Dual I/O” (BB hex) instruction. This instruction allows data to be transferred to or from the device at three to four the rate ordinary Serial Flash devices. The Dual Read instruction is ideal for quickly downloading code to RAM upon power-up (code-shadowing) or for executing non-speed-critical code directly from the SPI bus (XIP). When using Dual SPI instructions the DI and DO pins become bidirectional I/0 pins; IO0 and IO1.

### 10.1.3 Quad SPI Instructions

The FM25Q64 supports Quad SPI operation when using the “Fast Read Quad I/O” (EB hex). This instruction allows data to be transferred to or from the device six to seven times the rate of ordinary Serial Flash. The Quad Read instruction offers a significant improvement in continuous and random access transfer rates allowing fast code-shadowing to RAM or execution directly from the SPI bus (XIP). When using Quad SPI instruction the DI and DO pins become bidirectional IO0 and IO1, and the /WP and /HOLD pins become IO2 and IO3 respectively. Quad SPI instructions require the non-volatile Quad Enable bit (QE) in Status Register-2 to be set.

### 10.1.4 Hold Function

The /HOLD pin is used to pause a serial sequence of the SPI flash memory without resetting the clocking sequence. To activate the /HOLD mode, the /CS must be in active low state. The /HOLD mode begins when the CLK in active low state coincides with the falling edge of the /HOLD signal. The HOLD mode ends when the /HOLD signal’s rising edge coincides with the CLK in active low state.

If the falling edge of the /HOLD signal does not coincide with the CLK in active low state, then the device enters HOLD mode when the CLK reaches the next active low state. Similarly, if the rising edge of the /HOLD signal does not coincide with the CLK in active low state, then the device exits in HOLD mode when the CLK reaches the next active low state. See Figure.2 for HOLD condition waveform.

If /CS is driven active high during a HOLD condition, it resets the internal logic of the device. As long as /HOLD signal is low, the memory remains in the HOLD condition. To resume communication with the device, /HOLD must be driven active high, and /CS must be driven active low. See 12.11 for HOLD timing.

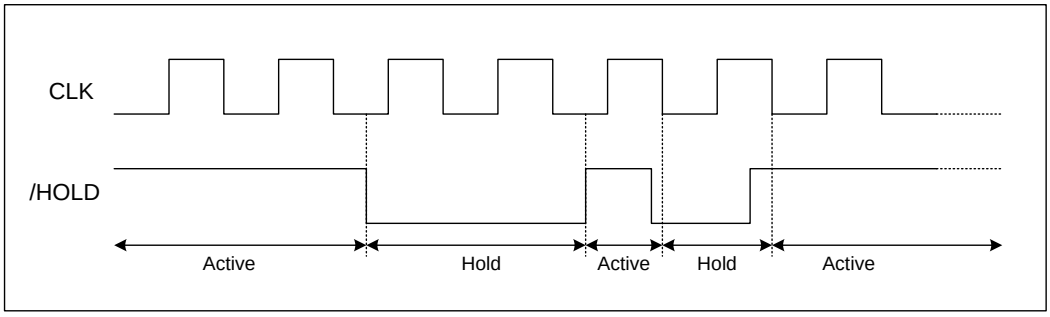



Figure2. Hold condition waveform

## 10.2 WRITE PROTECTION

Applications that use non-volatile memory must take consideration the possibility of noise and other adverse system conditions that may compromise data integrity. To address this concern the FM25Q64 provides several means to protect data from inadvertent writes.

### 10.2.1 Write protect Features

- Device resets when VCC is below threshold
- Time delay write disable after Power-up
- Write enable/disable instructions and automatic write disable after program and erase
- Software and Hardware (/WP pin) write protection using Status Register
- Write Protection using Power-down instruction
- Lock Down write protection until next power-up
- One Time Program (OTP) write protection

Upon power-up at power down the FM25Q64 will maintain a reset condition while VCC is below the threshold value of VWI, (See Power-up Timing and Voltage Levels and Figure 30). While reset, all operations are disabled and no instruction is recognized. During power-up and after the VCC voltage exceeds VWI, instructions related with all program and erase are further disabled for a time delay of tPUW. This includes the write Enable, Page program, Sector Erase, Block Erase, Chip Erase, Write Security Register and the Write Status Register instructions. Note that the chip select pin (/CS) must track the VCC supply level at power-up until the VCC-min level and tVSL time delay is reached. If needed a pull-up resister on /CS can be used to accomplish this.

After power-up the device is automatically placed in a write-disabled state with Status Register Write Enable Latch (WEL) set to a 0. A Write Enable instruction must be issued before a Page program, Sector Erase Chip Erase or Write Status Register and then instructions will be accepted. After completing a program, erase or write instruction the write Enable (WEL) is automatically cleared to write-disabled state of 0.

Software controlled write protection is facilitated using the Write Status Register instruction and setting the Status Register protect (SRP) and Block protect (SEC, TB, BP2, BP1, and BP0) bits. These setting allow a portion or all the memory to be configured as read only. Used in conjunction with the Write Protect (/WP) pin, changes to the Status Register can be enabled or disabled under hardware control. See Status Register for further information. Additionally, the Power-down instruction offers an extra level of write protection as all instructions are ignored except for Release power-down instruction.

# 11. CONTROL AND STATUS REGISTER

The Read Status Register instruction can be used to provide status on the availability of the Flash memory array, if the device is write enabled or disabled, the state of write protection and the Quad SPI setting. The Write Status Register instruction can be used to configure the devices write protection features and Quad SPI setting. Write access to the Status Register is controlled by in some cases of the /WP pin.

## 11.1 STATUS REGISTER

### 11.1.1 BUSY

BUSY is a read only bit in the status register (S0) that is set to a 1 state when the device is executing a Page Program, Sector Erase, Block Erase, Chip Erase or Write Status Register instruction. During this time the device will ignore further instruction except for the Read Status Register and Erase Suspend instruction (see tW, tPP, tSE, tBE1, tBE2 and tCE in AC Characteristics). When the program, erase or write status register instruction has completed, the BUSY bit will be cleared to a 0 state indicating the device is ready for further instructions.

### 11.1.2 Write Enable Latch (WEL)

Write Enable Latch (WEL) is a read only bit in the status register (S1) that is set to a 1 after executing a Write Enable instruction. The WEL status bit is cleared to a 0, When device is write disabled. A write disable state occurs upon power-up or after any of the following instructions: Write Disable, Page Program, Sector Erase, Block Erase, Chip Erase and Write Status Register.

### 11.1.3 Block Protect Bits (BP2, BP1, BP0)

The Block Protect Bits (BP2, BP1, BP0) are non-volatile read/write bits in the status register (S4, S3, and S2) that provide write protection control and status. Block protect bits can be set using the Write Status Register Instruction (see tW in AC characteristics). All none or a portion of the memory array can be protected from Program and Erase instructions (see Status Register Memory Protection table). The factory default setting for the Block Protection Bits is 0, none of the array protected.

### 11.1.4 Top/Bottom Block protect (TB)

The non-volatile Top/Bottom bit (TB) controls if the Block Protect Bits (BP2, BP1, BP0) protect from the Top (TB=0) or the Bottom (TB=1) of the array as shown in the Status Register Memory Protection table. The factory default setting is TB=0. The TB bit can be set with the Write Status Register Instruction depending on the state of the SRP0, SRP1 and WEL bits.

### 11.1.5 Sector/Block Protect (SEC)

The non-volatile Sector protect bit (SEC) controls if the Block Protect Bits (BP2, BP1, BP0) protect 4KB Sectors (SEC=1)or 64KB Blocks (SEC=0) in the Top (TB=0) or the Bottom (TB=1) of the array as shown in the Status Register Memory protection table. The default setting is SEC=0.

### 11.1.6 Status Register protect (SRP1, SRP0)

The Status Register Protect bits (SRP1 and SRP0) are non-volatile read/write bits in the status register (S8 and S7). The SRP bits control the method of write protection: software protection, hardware protection, power supply lock-down or one time programmable (OTP) protection.

| SRP1 | SRP0 | /WP | Status Register | Description |
|---|---|---|---|---|
| 0 | 0 | X | Software Protection | /WP pin no control. The register can be written to after a Write Enable instruction, WEL=1. [Factory Default] |
| 0 | 1 | 0 | Hardware Protected | When /WP pin is low the Status Register locked and can not be written to. |
| 0 | 1 | 1 | Hardware Unprotected | When /WP pin is high the Status register is unlocked and can be written to after a Write Enable instruction, WEL=1 |
| 1 | 0 | X | Power Supply Lock-Down | Status Register is protected and can not be written to again until the next power-down, power-up cycle(1). |
| 1 | 1 | X | One Time Program | Status Register is permanently protected and can not be written to. |

Note:

1. When SRP1, SRP0=(1,0), a power-down, power-up cycle will change SRP1, SRP0 to(0,0) state.

### 11.1.7 Erase/Program Suspend Status (SUS)

The Suspend Status bit is a read only bit in the status register (S15) that is set to 1 after executing an Erase/Program Suspend (75h) instruction. The SUS status bit is cleared to 0 by Erase/Program Resume (7Ah) instruction as well as a power-down, power-up cycle.

### 11.1.8 Quad Enable (QE)

The Quad Enable (QE) bit is a non-volatile read/write bit in the status register (S9) that allows Quad operation. When the QE bit is set to a 0 state (factory default) the /WP pin and /Hold are enabled. When the QE pin is set to a 1 the Quad IO2 and IO3 pins are enabled.

**WARNING : The QE bit should never be set to a 1 during standard SPI or Dual SPI operation if the /WP or /HOLD pins are tied directly to the power supply or ground.**

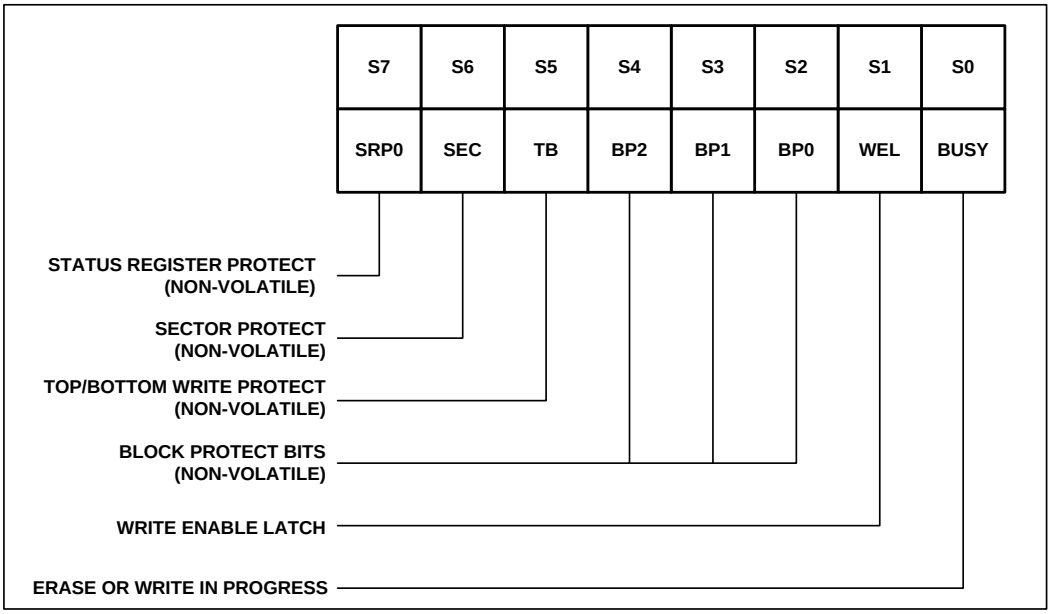



Figure 3a. Status Register-1

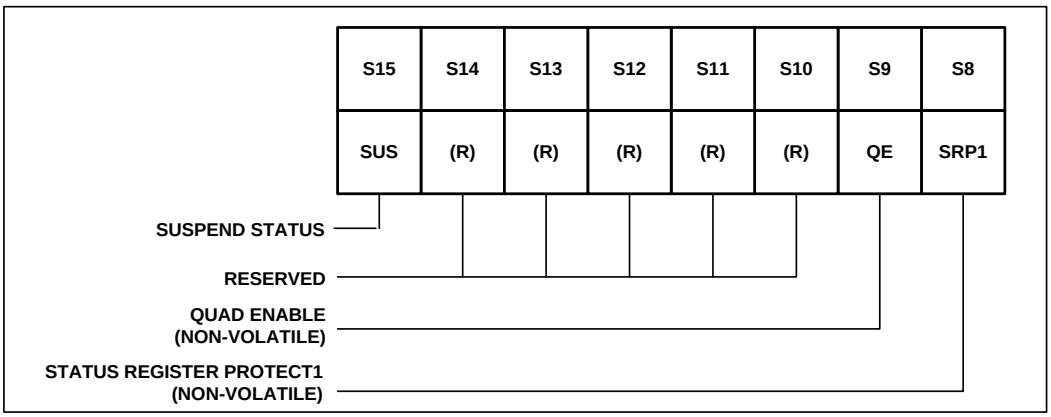



Figure 3b. Status Register-2

### 11.1.9 Status Register Memory Protection

| STATUS REGISTER[1] | | | | | MEMORY PROTECTION | | | |
|---|---|---|---|---|---|---|---|---|
| SEC | TB | BP2 | BP1 | BP0 | BLOCK(S) | ADDRESSES | DENSITY | PORTION |
| X | X | 0 | 0 | 0 | NONE | NONE | NONE | NONE |
| 0 | 0 | 0 | 0 | 1 | 126 and 127 | 7E0000h-7FFFFFh | 128KB | Upper 1/64 |
| 0 | 0 | 0 | 1 | 0 | 124 thru 127 | 7C0000h-7FFFFFh | 256KB | Upper 1/32 |
| 0 | 0 | 0 | 1 | 1 | 120 thru 127 | 780000h-7FFFFFh | 512KB | Upper 1/16 |
| 0 | 0 | 1 | 0 | 0 | 112 thru 127 | 700000h-7FFFFFh | 1M | Upper 1/8 |
| 0 | 0 | 1 | 0 | 1 | 96 thru 127 | 600000h-7FFFFFh | 2MB | Upper 1/4 |
| 0 | 0 | 1 | 1 | 0 | 64 thru 127 | 400000h-7FFFFFh | 4MB | Upper 1/2 |
| 0 | 1 | 0 | 0 | 1 | 0 and 1 | 000000h-01FFFFh | 128KB | Lower 1/64 |
| 0 | 1 | 0 | 1 | 0 | 0 thru 3 | 000000h-03FFFFh | 256KB | Lower 1/32 |
| 0 | 1 | 0 | 1 | 1 | 0 thru 7 | 000000h-07FFFFh | 512KB | Lower 1/16 |
| 0 | 1 | 1 | 0 | 0 | 0 thru 15 | 000000h-0FFFFFh | 1MB | Lower 1/8 |
| 0 | 1 | 1 | 0 | 1 | 0 thru 31 | 000000h-1FFFFFh | 2MB | Lower 1/4 |
| 0 | 1 | 1 | 1 | 0 | 0 thru 63 | 000000h-3FFFFFh | 4MB | Lower 1/2 |
| X | X | 1 | 1 | 1 | 0 thru 127 | 000000h-7FFFFFh | 8MB | ALL |
| 1 | 0 | 0 | 0 | 1 | 127 | 7FF000h-7FFFFFh | 4KB | Top Block |
| 1 | 0 | 0 | 1 | 0 | 127 | 7FE000h-7FFFFFh | 8KB | Top Block |
| 1 | 0 | 0 | 1 | 1 | 127 | 7FC000h-7FFFFFh | 16KB | Top Block |
| 1 | 0 | 1 | 0 | X | 127 | 7F8000h-7FFFFFh | 32KB | Top Block |
| 1 | 1 | 0 | 0 | 1 | 0 | 000000h-000FFFh | 4KB | Bottom Block |
| 1 | 1 | 0 | 1 | 0 | 0 | 000000h-001FFFh | 8KB | Bottom Block |
| 1 | 1 | 0 | 1 | 1 | 0 | 000000h-003FFFh | 16KB | Bottom Block |
| 1 | 1 | 1 | 0 | X | 0 | 000000h-007FFFh | 32KB | Bottom Block |

Note :
1. X = don't care

## 11.2 INSTRUCTIONS

The instruction set of the FM25Q64 consists of fifteen basic instructions that are fully controlled through the SPI bus (see Instruction Set table). Instructions are initiated with the falling edge of Chip Select (/CS). The first byte of data clocked into the DI input provides the instruction code. Data on the DI input is sampled on the rising edge of clock with most significant bit (MSB) first.

Instructions vary in length from a single byte to several bytes and may be followed by address bytes, data bytes, dummy bytes (don't care), and in some cases, a combination. Instructions are completed with the rising edge of edge /CS. Clock relative timing diagrams for each instruction are included in figures 4 through 29. All read instructions can be completed after any clocked bit. However, all instructions that Write, Program or Erase must complete on a byte (/CS driven high after a full 8-bit have been clocked) otherwise the instruction will be terminated. This feature further protects the device from inadvertent writes. Additionally, while the memory is being programmed or erased, or when the Status Register is being written, all instructions except for Read Register will be ignored until the program or erase cycle has completed.

### 11.2.1 Manufacturer and Device Identification

| | | |
|---|---|---|
| **MANUFACTRER ID** | **(M7-M0)** | |
| Fidelix Semiconductor | F8h | |
| | | |
| **Device ID** | **(ID7-ID0)** | **(ID15-ID0)** |
| **Instruction** | **ABh, 90h** | **9Fh** |
| FM25Q64 | 16h | 3217h |

### 11.2.2 Instruction Set Table 1[1]

| INSTRUCTION NAME | BYTE 1 (CODE) | BYTE 2 | BYTE 3 | BYTE 4 | BYTE 5 | BYTE 6 |
|---|---|---|---|---|---|---|
| Write Enable | **06h** | | | | | |
| Write Enable for Volatile Status Register | **50h** | | | | | |
| Write Disable | **04h** | | | | | |
| Read Status Register-1 | **05h** | (S7-S0) [2] | | | | |
| Read Status Register-2 | **35h** | (S15-S8)[2] | | | | |
| Write Status Register | **01h** | (S7-S0) | (S15-S8) | | | |
| Page Program | **02h** | A23-A16 | A15-A8 | A7-A0 | (D7-D0) | |
| Quad Data Input Page Program[3] | **32h** | A23-A16 | A15-A8 | A7-A0 | (D7-D0, …)[3] | |
| Quad Page Program | **38h** | A23-A0, (D7-D0) | A15-A8 | A7-A0 | (D7-D0, …)[3] | |
| Block Erase (64KB) | **D8h** | A23-A16 | A15-A8 | A7-A0 | | |
| Block Erase (32KB) | **52h** | A23-A16 | A15-A8 | A7-A0 | | |
| Sector Erase (4KB) | **20h** | A23-A16 | A15-A8 | A7-A0 | | |
| Chip Erase | **C7h/60h** | | | | | |
| Erase Suspend | **75h** | | | | | |
| Erase Resume | **7Ah** | | | | | |
| Power-down | **B9h** | | | | | |
| Mode Bit Reset[4] | **FFh** | | | | | |
| Release power down/ Device ID | **ABh** | dummy | dummy | dummy | (ID7-ID0) [5] | |
| Read Manufacturer/ Device ID[6] | **90h** | dummy | dummy | 00h or 01h | (M7-M0) | (ID7-ID0) |
| Read Dual Manufacturer/ Device ID[6] | **EFh** | dummy | dummy | 00h or 01h | (M7-M0) (ID7-ID0) | |
| Read Quad Manufacturer/ Device ID[6] | **DFh** | dummy | dummy | 00h or 01h | (M7-M0…) (ID7-ID0…) | |
| Write Security Register | **2Fh** | | | | | |
| Read Security Register | **2Bh** | (S7-S0) | | | | |
| Enter Secured OTP | **B1h** | | | | | |
| Exit Secured OTP | **C1h** | | | | | |
| Read JEDEC ID | **9Fh** | (M7-M0) Manufacturer | (ID7-ID0) Memory Type | (ID7-ID0) Capacity | | |

**Notes:**

1. Data bytes are shifted with Most Significant Bit first. Byte fields with data in parenthesis "()" indicate data being read from the device on the IO pin.

2. The Status Register contents will repeat continuously until /CS terminates the instruction.
3. Quad Data Input Page Program Input Data
   IO0 = (D4, D0 …)
   IO1 = (D5, D1 …)
   IO2 = (D6, D2 …)
   IO3 = (D7, D3 …)
4. This instruction is recommended when using the Dual or Quad Mode bit feature. See section 10.2.28 for more information.
5. The Device ID will repeat continuously until /CS terminates the instruction.
6. See Manufacturer and Device Identification table for Device ID information.

### 11.2.3 Instruction Set Table 2 (Read Instructions)

| INSTRUCTION NAME | BYTE 1 (CODE) | BYTE 2 | BYTE 3 | BYTE 4 | BYTE 5 | BYTE 6 |
|---|---|---|---|---|---|---|
| Read Data | **03h** | A23-A16 | A15-A8 | A7-A0 | (D7-D0) | |
| Fast Read Data | **0Bh** | A23-A16 | A15-A8 | A7-A0 | dummy | (D7-D0) |
| Fast Read Dual I/O | **BBh** | A23-A8(2) | A7-A0, M7-M0(2) | (D7-D0, …)(1) | | |
| Fast Read Quad I/O | **EBh** | A23-A0, M7-M0(4) | (x,x,x,x, D7-D0,…)(5) | (D7-D0, …)(3) | | |
| Set Burst with Wrap | **77h** | xxxxxx, W6-W4(4) | | | | |

Notes:

1: Dual Output data
IO0 = (D6, D4, D2, D0)
IO1 = (D7, D5, D3, D1)

2: Dual Input Address
IO0 = A22, A20, A18, A16, A14, A12, A10, A8, A6, A4, A2, A0, M6, M4, M2, M0
IO1 = A23, A21, A19, A17, A15, A13, A11, A9, A7, A5, A3, A1, M7, M5, M3, M1

3: Quad Output Data
IO0 = (D4, D0…)
IO1 = (D5, D1…)
IO2 = (D6, D2…)
IO3 = (D7, D3…)

4: Quad Input Address

IO0 = A20, A16, A12, A8, A4, A0, M4, M0
IO1 = A21, A17, A13, A9, A5, A1, M5, M1
IO2 = A22, A18, A14, A10, A6, A2, M6, M2
IO3 = A23, A19, A15, A11, A7, A3, M7, M3

Set Burst with Wrap Input
IO0 = x, x, x, x, x, x, W4, x
IO1 = x, x, x, x, x, x, W5, x
IO2 = x, x, x, x, x, x, W6, x ,
IO3 = x, x, x, x, x, x x

5: Fast Read Quad I/O Data
IO0 = (x, x, x, x, D4, D0…)
IO1 = (x, x, x, x, D5, D1…)
IO2 = (x, x, x, x, D6, D2…)
IO3 = (x, x, x, x, D7, D3…)

### 11.2.4 Write Enable (06h)

The Write Enable instruction (Figure 4) sets the Write Enable Latch (WEL) bit in the Status Register to a 1. The WEL bit must be set prior to every Page Program, Sector Erase, Block Erase, Chip Erase and Write Status Register instruction. The Write Enable instruction is entered by driving /CS low, shifting the instruction code "06h" into Data Input (DI) pin on the rising edge of CLK, and then driving /CS high.

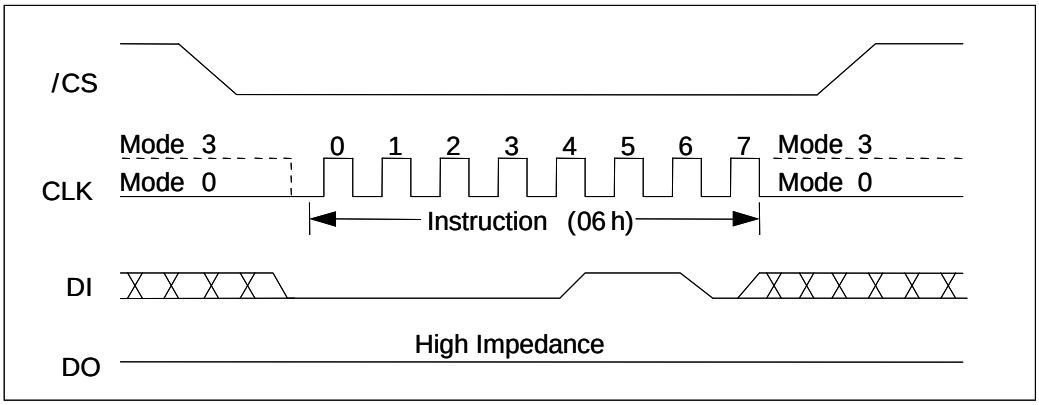



Figure 4. Write Enable Instruction Sequence Diagram

### 11.2.5 Write Enable for Volatile Status Register (50h)

The non-volatile Status Register bits described in section 12.1 can also be written to as volatile bits. This gives more flexibility to change the system configuration and memory protection schemes quickly without waiting for the typical non-volatile bit write cycles or affecting the endurance of the Status Register non-volatile bits. To write the volatile values into the Status Register bits, the Write Enable for Volatile Status Register (50h) instruction must be issued prior to a Write Status Register (01h) instruction. Write Enable for Volatile Status Register instruction (Figure 5) will not set the Write Enable Latch (WEL) bit, it is only valid for the Write Status Register instruction to change the volatile Status Register bit values

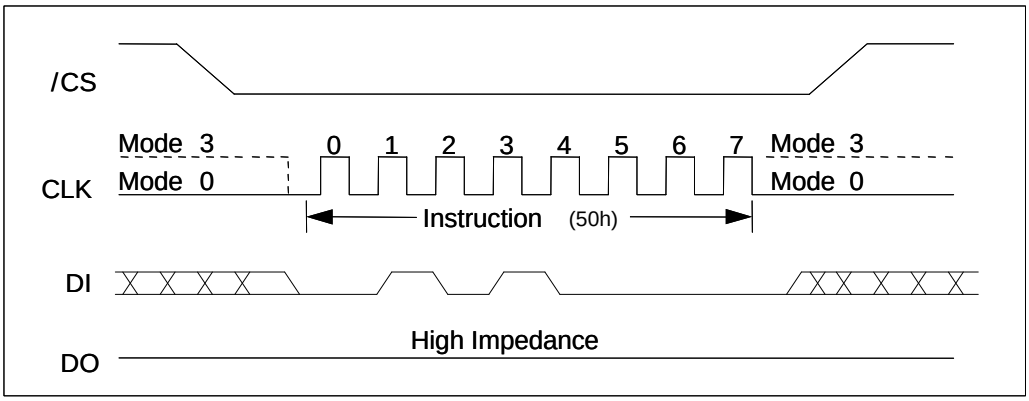



Figure 5. Write Enable for Volatile Status Register Instruction Sequence Diagram

### 11.2.6 Write Disable (04h)

The Write Disable instruction (Figure 6) resets the Write Enable Latch (WEL) bit in the Status Register to a 0. The Write Disable instruction in entered by driving /CS low, shifting the instruction code “04h” into the DI pin and then driving /CS high. Note that the WEL bit is automatically reset after Power-up and upon completion of the Write Status Register, Page Program, Sector Erase, Block Erase and Chip Erase instructions. .

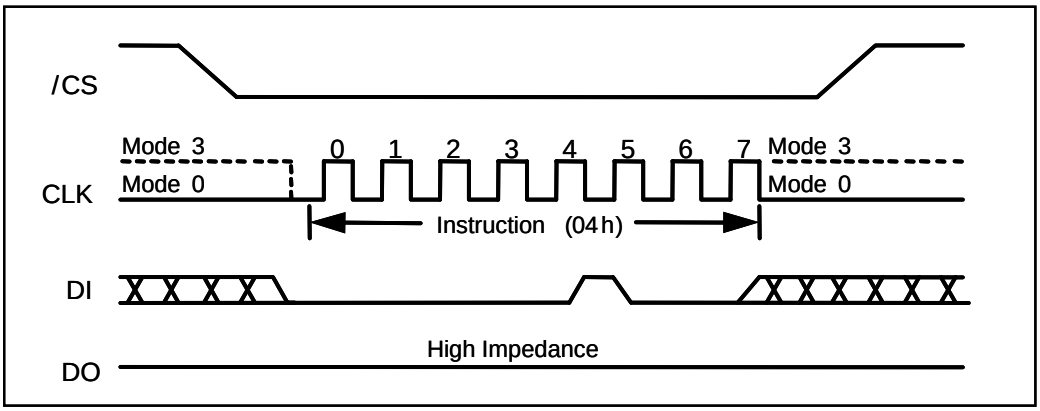



Figure 6. Write Disable Instruction Sequence Diagram

### 11.2.7 Read Status Register-1 (05h) and Read Status Register-2 (35h)

The Read Status Register instructions allow the 8-bit Status Register to be read, The instruction is entered by driving /CS low and shifting the instruction code “05h” for Status Register-1 and “35h” for Status Register-2 into the DI pin on the rising edge of CLK. The status register bits are then shifted out on the DO pin at the falling edge of CLK with most significant bit (MSB) first as shown in figure 7. The Status Register bits are shown in figure 3a and 3b include the BUSY, WEL, BP2-BP0, TB, SEC, SRP0, SRP1 and QE bits (see description of the Status Register earlier in this datasheet).

The Status Register instruction may be used at any time, even while a Program, Erase, Write Security Register or Write Status Register cycle is in progress. This allows the BUSY status bit to be checked to determine when the cycle is complete and if the device can accept another instruction. The Status Register can be read continuously, as shown in Figure 7. The instruction is completed by driving /CS high.

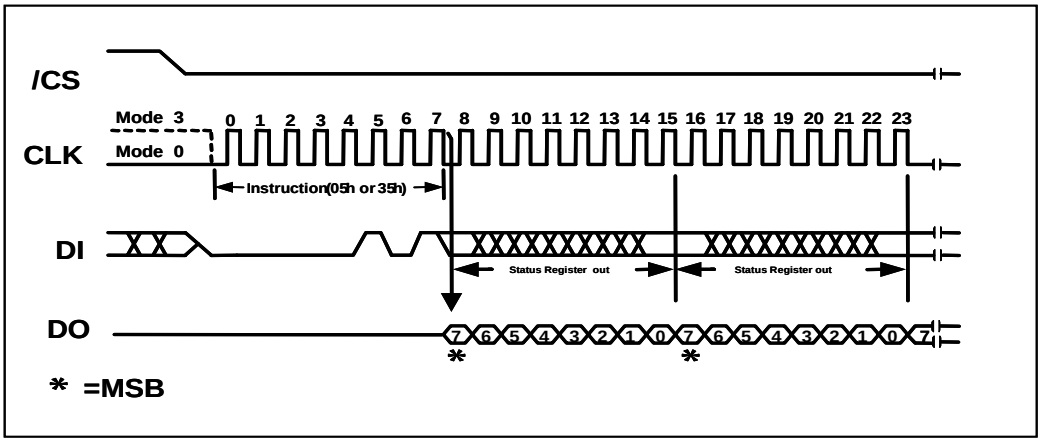



Figure 7. Read Status Register Instruction Sequence Diagram

### 11.2.8 Write Status Register (01h)

The Write Status Register instruction allows the Status Register to be written. A Write Enable instruction must previously have been executed for the device to accept the Write Status Register Instruction (Status Register bit WEL must equal 1). Once write is enabled, the instruction is entered by driving /CS low, sending the instruction code “01h”, and then writing the status register data byte or word as illustrated in figure 8. The Status Register bits are shown in figure 3 and described earlier in this datasheet.

Only non-volatile Status Register bits SRP0, SEC, TB, BP2, BP1, BP0 (bits 7, 5, 4, 3, 2 of Status Register-1) and QE, SRP1 (bits 9 and 8 of Status Register-2) can be written to. All other Status Register bit locations are read-only and will not be affected by the Write Status Register instruction.

The /CS pin must be driven high after the eighth or sixteenth bit of data that is clocked in. If this is not done the Write Status Register instruction will not be executed. If /CS is driven high after the eighth clock, the QE and SRP1 bits will be cleared to 0. After /CS is driven high, the self-timed Write Status Register cycle will commence for a time duration of tw (See AC Characteristics). While the Write Status Register cycle is in progress, the Read Status Register instruction may still be accessed to check the status of the BUSY bit. The BUSY bit is a 1 during the Write Status Register cycle and a 0 when the cycle is finished and ready to accept other instructions again. After the Write Status Register cycle has finished, The Write Enable Latch (WEL) bit in Status Register will be cleared to 0.

The Write Status Register instruction allows the Block Protect bits (SEC, TB, BP2, BP1 and BP0) to be set for protecting all, a portion, or none of the memory from erase and program instructions. Protected areas become read-only (see Status Register Memory Protection table and description). The Write Status Register instruction also allows the Status Register Protect bits (SRP0, SRP1) to be set. Those bits are used in conjunction with the Write protect (/WP) pin, Lock out or OTP features to disable writes to the status register. Please refer to 11.1.16 for detailed descriptions Status Register protection methods. Factory default all Status Register bits are 0.

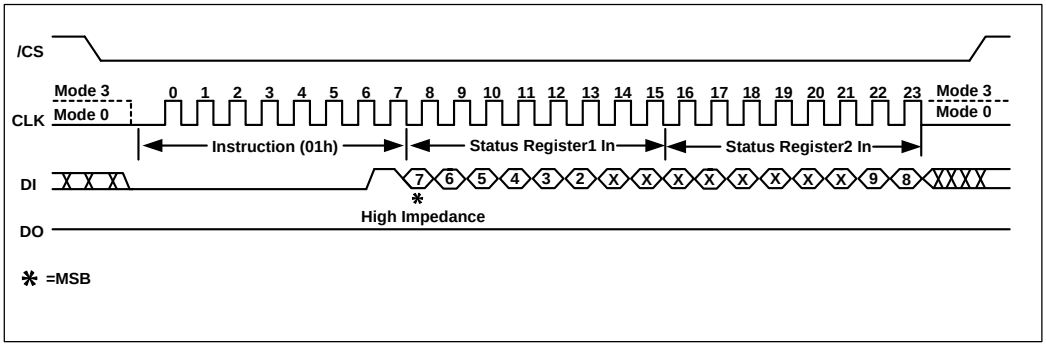



Figure 8. Write Status Register Instruction Sequence Diagram

### 11.2.9 Read Data (03h)

The Read Data instruction allows one more data bytes to be sequentially read from the memory. The instruction is initiated by driving the /CS pin low and then shifting the instruction code “03h” followed by a 24-bit address (A23-A0) into the DI pin. The code and address bits are latched on the rising edge of the CLK pin. After the address is received, the data byte of the addressed memory location

will be shifted out on the DO pin at the falling edge of CLK with most significant bit (MSB) first. The address is automatically incremented to the next higher address after byte of data is shifted out allowing for a continuous stream of data. This means that the entire memory can be accessed with a single instruction as long as the clock continues. The instruction is completed by driving /CS high. The Read Data instruction sequence is shown in figure 9. If a Read Data instruction is issued while an Erase, Program or Write Status Register cycle is in process (BUSY=1) the instruction is ignored and will not have any effects on the current cycle. The Read Data instruction allows clock rates from D.C to a maximum of $f_R$ (see AC Electrical Characteristics).

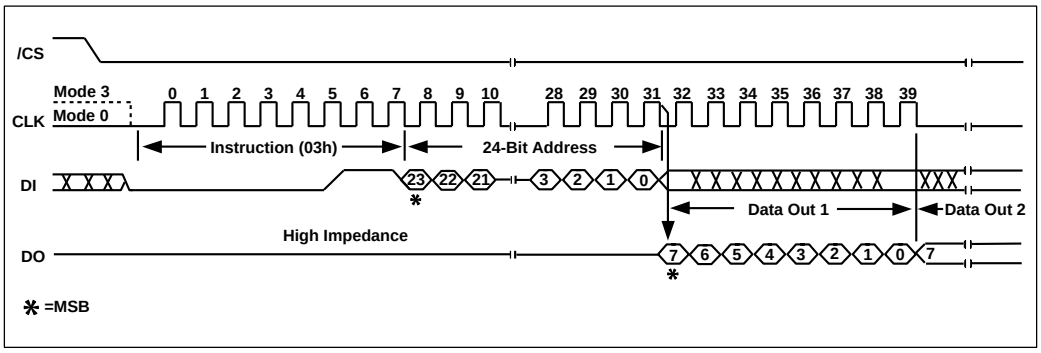



Figure 9. Read Data Register Instruction Sequence Diagram

### 11.2.10 Fast Read (0Bh)

The Fast Read instruction is similar to the Read Data instruction except that it can operate at the highest possible frequency of $F_R$ (see AC Electrical Characteristics). This is accomplished by adding eight "dummy" clocks after the 24-bit address as shown in figure 10. The dummy clocks allow the device's internal circuits additional time for setting up the initial address. During the dummy clocks, The data value on the DO pin is a "don't care".

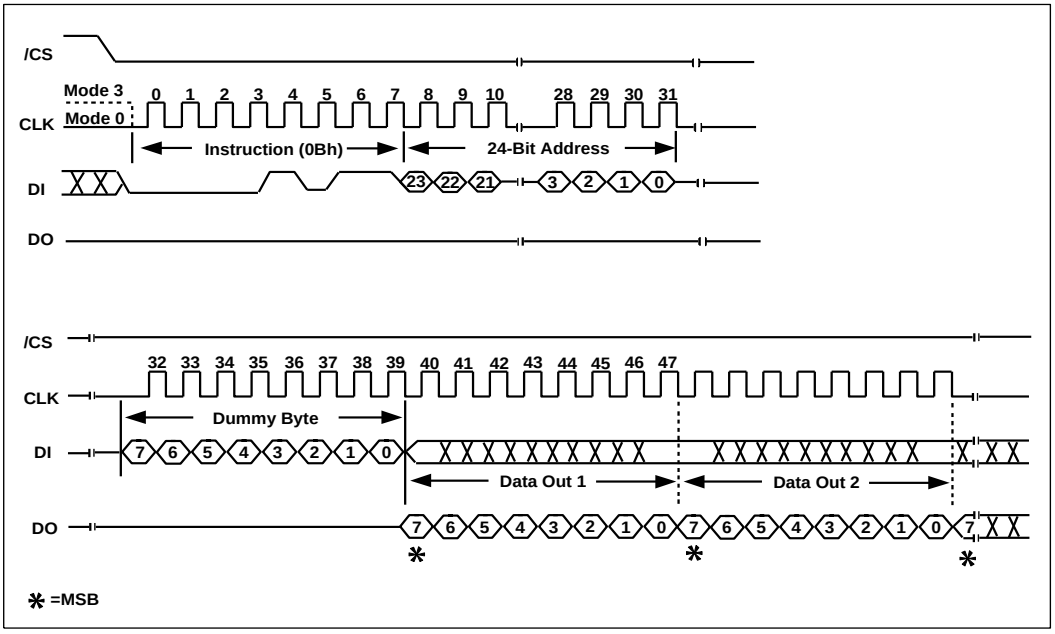



Figure 10. Fast Read Register Instruction Sequence Diagram

### 11.2.11 Fast Read Dual I/O (BBh)

The Fast Read Dual I/O (BBh) instruction allows for improved random access while maintaining two IO pins, $IO_0$ and $IO_1$. It is similar to the Fast Read Output (0Bh) instruction but with the capability to input the Address bits (A23-0) two bits and output data two bits per clock. This reduced instruction overhead may allow for code execution (XIP) directly from the Dual SPI in some applications.

The Fast Read Dual I/O instruction can further reduce instruction overhead through setting the Mode bits (M7-0) after the input Address bits (A23-0), as shown in figure 11a. The upper nibble of the Mode (M7-4) controls the length of the next Fast Read Dual I/O instruction through the instruction or exclusion of the first byte instruction code. The lower nibble bits of the Mode (M3-0) are don't care ("X"), However, the IO pins should be high-impedance prior to the falling edge of the first data out clock.

If the Mode bits (M7-0) equal "Ax" hex, then the next Fast Dual I/O instruction (after /CS is raised and then lowered) does not require the BBh instruction code, as shown in figure 11b. This reduces the instruction sequence by eight clocks and allows the address to be immediately entered after /CS is asserted low. If Mode bits (M7-0) are any value other "Ax" hex, the next instruction (after /CS is raised and then lowered) requires the first byte instruction code, thus returning to normal operation. A Mode Bit Reset instruction can be used to reset Mode Bits (M7-0) before issuing normal instructions (See 11.2.25 for detailed descriptions).

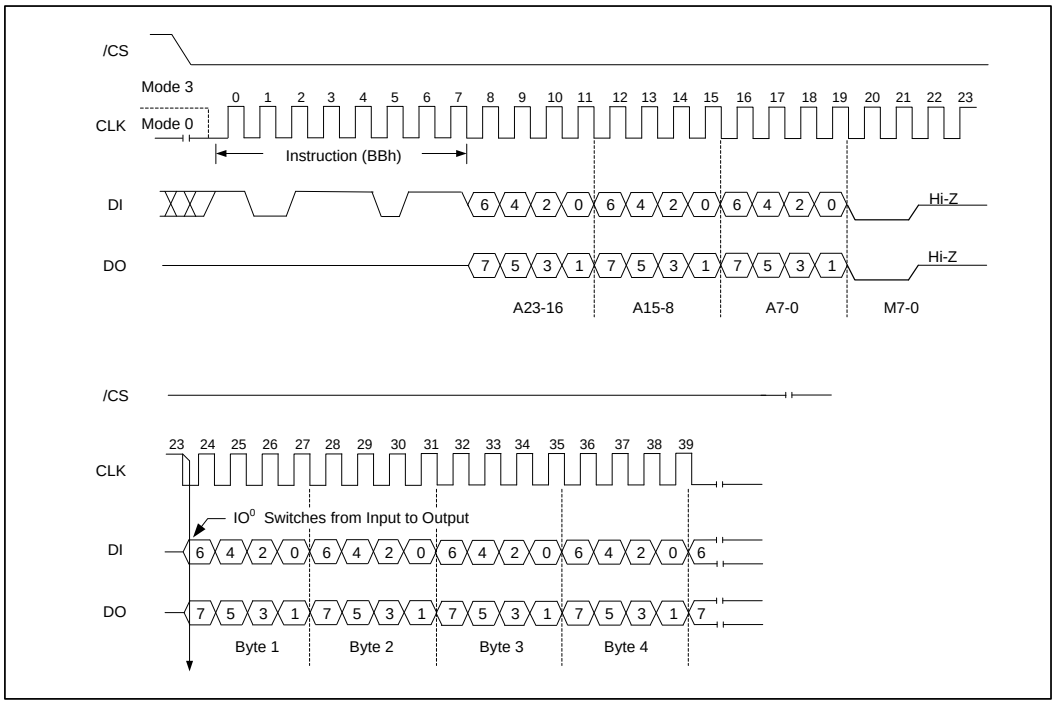



Figure 11a. Fast Read Dual Input/Output Instruction Sequence Diagram (M7-0 = 0xh or NOT Axh)

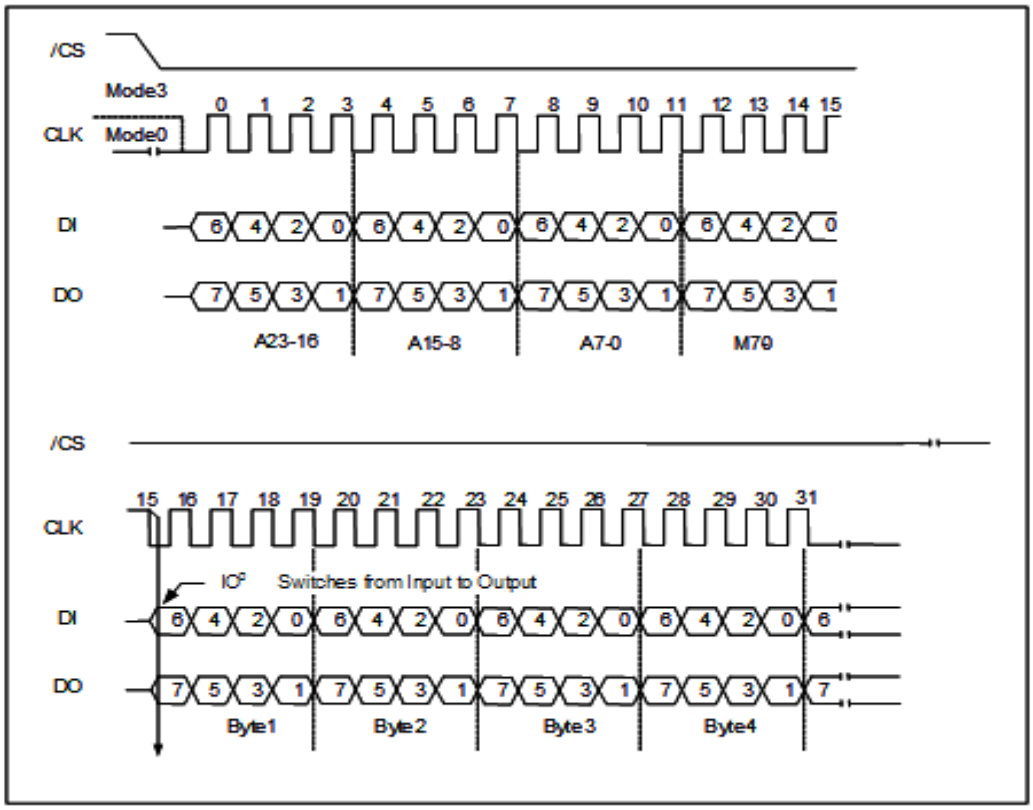



Figure 11b. Fast Read Dual Input/Output Instruction Sequence Diagram (M7-0 = Axh)

### 11.2.12 Fast Read Quad I/O (EBh)

The Fast Read Quad I/O (EBh) instruction is similar to the Fast Read Dual I/O (BBh) instruction except that address and data bits are input and output through four pins $IO_0$, $IO_1$, $IO_2$, and $IO_3$ and four Dummy clock are required prior to the data output. The Quad I/O dramatically reduces instruction overhead allowing faster random access for code executing (XIP) directly from the Quad SPI. The Quad Enable bit (QE) of Status Register-2 must be set to enable the Fast read Quad I/O Instruction.

The Fast Read Quad I/O instruction can further reduce instruction overhead through setting the Mode bits (M7-0) after the input Address bits (A23-0), as shown in figure 12a. The upper nibble of the Mode (M7-4) controls the length of the next Fast Read Quad I/O instruction through the instruction or exclusion of the first byte instruction code. The lower nibble bits of the Mode (M3-0) are don't care ("X"). However, the IO pins should be high-impedance prior to the falling edge of the first data out clock.

If the Mode bits (M7-0) equal "Ax" hex, then the next Fast Read Quad I/O instruction (after /CS is raised and then lowered) does not require the EBh instruction code, as shown in figure 12b. This reduces the instruction sequence by eight clocks allows the address to be immediately entered after /CS is asserted low. If the Mode bits (M7-0) are any value other than "Ax" hex, the next instruction (after /CS is raised and then lowered) requires the first byte instruction code, thus retuning normal operation. A Mode Bit Reset can be used to reset Mode Bits (M7-0) before issuing normal instructions (See 11.2.25 for detailed descriptions.)

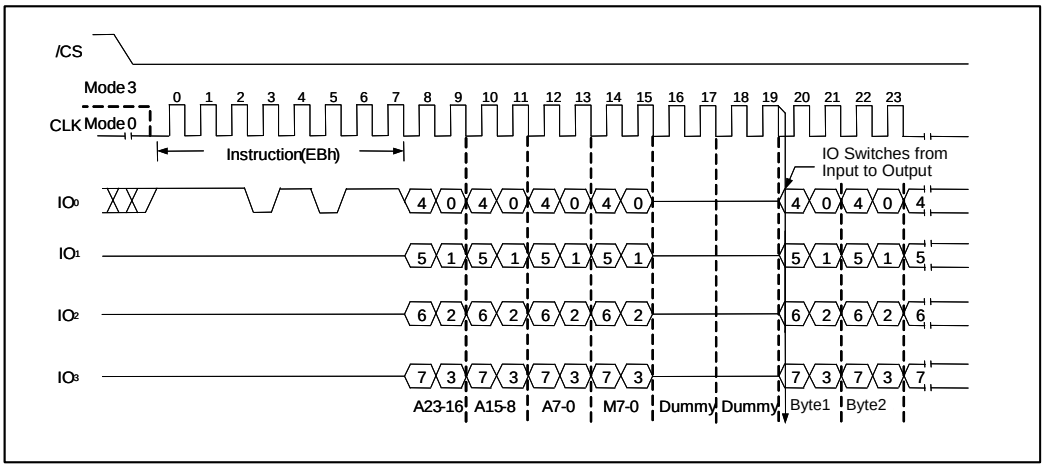



Figure 12a. Fast Read Quad Input/Output Instruction Sequence Diagram (M7-0 = 0xh or NOT Axh)

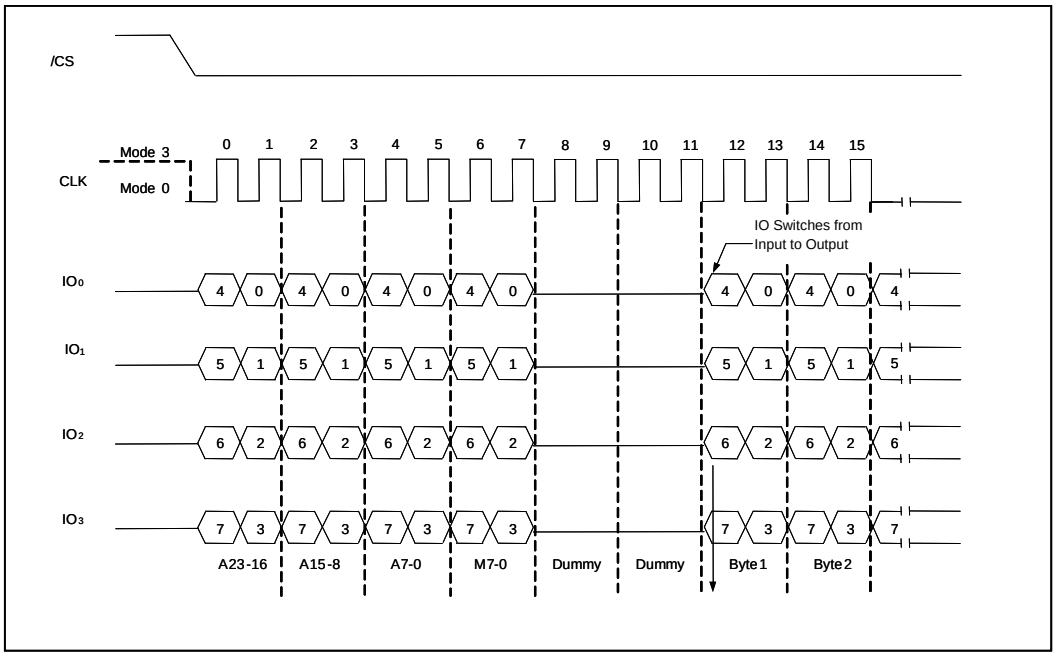



Figure 12b. Fast Read Quad Input/Output Instruction Sequence Diagram (M7-0 = Axh)

### 11.2.13 Page Program (02h)

The Page Program instruction allows from one byte to 256 bytes (a page) of data to be programmed at previously erased (FFh) memory locations. A Write Enable instruction must be executed before the device will accept the Page Program Instruction (Status Register bit WEL= 1). The instruction is initiated by driving the /CS pin low and then shifting the instruction code “02h” followed by a 24-bits address (A23-A0) and at least one data byte, into the DI pin. The /CS pin must be held low for the entire length of the instruction while data is being sent to the device. The Page Program instruction sequence is shown is figure 13.

If an entire 256 byte page is to be programmed, the last address byte (the 8 least significant address bits) should be set to 0. If the last address byte is not zero, and the number of clocks exceeds the remaining page length, the addressing will wrap to the beginning of the page. In some cases, less than 256 bytes (a partial page) can be programmed without having any effect on other bytes within the same page. One condition to perform a partial page program is that the number of clocks can not exceed the remaining page length. If more than 256 bytes are sent to the device the addressing will wrap to the beginning of the page and overwrite previously sent data.

As with the write and erase instructions, the /CS pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Page Program instruction will not be executed. After /CS is driven high, the self-timed Page Program instruction will commence for a time duration of tPP (See AC Characteristics). While the Page Program cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the Page Program cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Page Program cycle has finished and Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Page Program instruction will not be executed if the addressed page is protected by the Block Protect (SEC, TB, BP2, BP1, and BP0) bits,

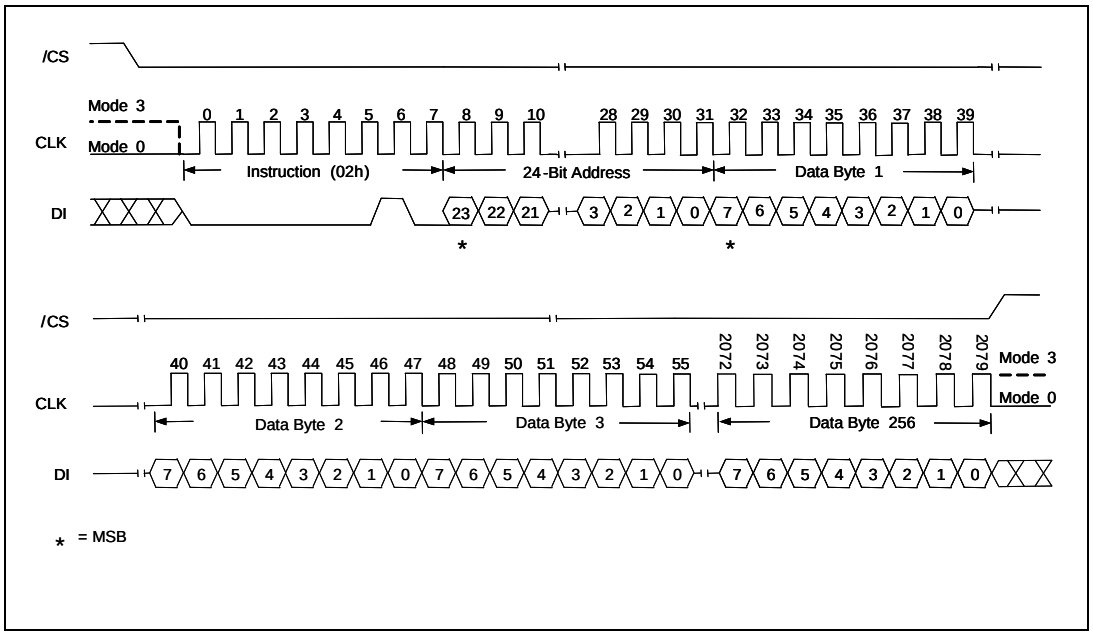



Figure 13. Page Program Instruction Sequence Diagram

### 11.2.14 Quad Data Input Page Program (32h)

The Quad Data Input Page Program instruction allows up to 256 bytes of data to be programmed at previously erased (FFh) memory locations using four pins: $IO_0$, $IO_1$, $IO_2$ and $IO_3$. The Quad Data Input Page Program can improve performance for PROM Programmer and applications that have slow clock speed <5MHz. System with faster clock speed will not realize much benefit for the Quad Data Input Program instruction since the inherent page program time is much greater than the time it takes to clock-in the data.

To use Quad Data Input Page Program the Quad Enable in Status Register-2 must be set (QE=1), A Write Enable instruction must be executed before the device will accept the Quad Data Input Page Program instruction (Status Register-1, WEL=1). The instruction is initiated by driving the /CS pin low and then shifting the instruction code “32h” followed by a 24-bit address (A23-A0) and at least one data, into the IO pins. The /CS pin must be held low for the entire length of the instruction while data is being sent to the device. All other functions of Quad Data Input Page Program are identical standard Page Program. The Quad Data Input Page Program instruction sequence is shown in figure 14.

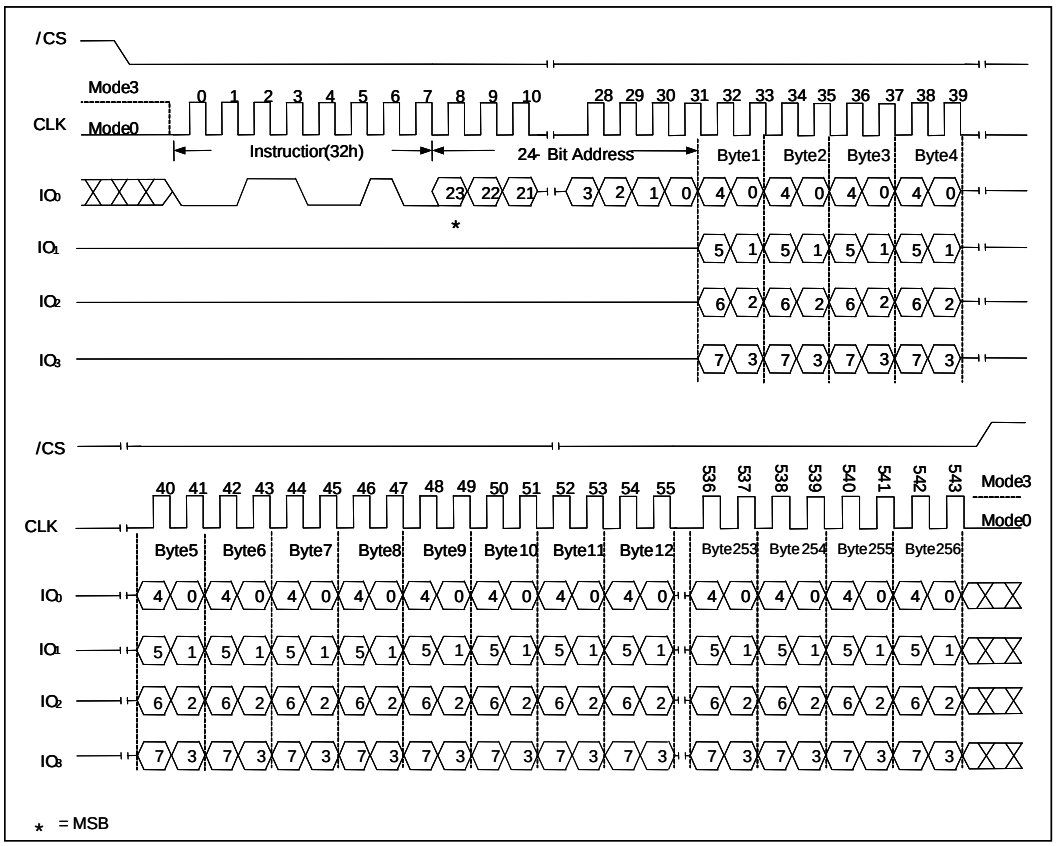



Figure 14. Quad Data Input Page Program Instruction Sequence Diagram

### 11.2.15 Quad Page Program (38h)

The Quad Page Program instruction allows 24-bit address and up to 256 bytes of data to be programmed at previously erased (FFh) memory locations using four pins: $IO_0$, $IO_1$, $IO_2$ and $IO_3$. The Quad Page Program can improve performance for PROM Programmer and applications that have slow clock speed <5MHz. System with faster clock speed will not realize much benefit for the Quad Page Program instruction since the inherent page program time is much greater than the time it takes to clock-in the data.

To use Quad Page Program the Quad Enable in Status Register-2 must be set (QE=1), A Write Enable instruction must be executed before the device will accept the Quad Page Program instruction (Status Register-1, WEL=1). The instruction is initiated by driving the /CS pin low then shifting the instruction code "38h" followed by a 24-bit address (A23-A0) and at least one data, into the IO pins. The /CS pin must be held low for the entire length of the instruction while data is being sent to the device. All other functions of Quad Page Program are identical standard Page Program. The Quad Page Program instruction sequence is shown in figure 15.

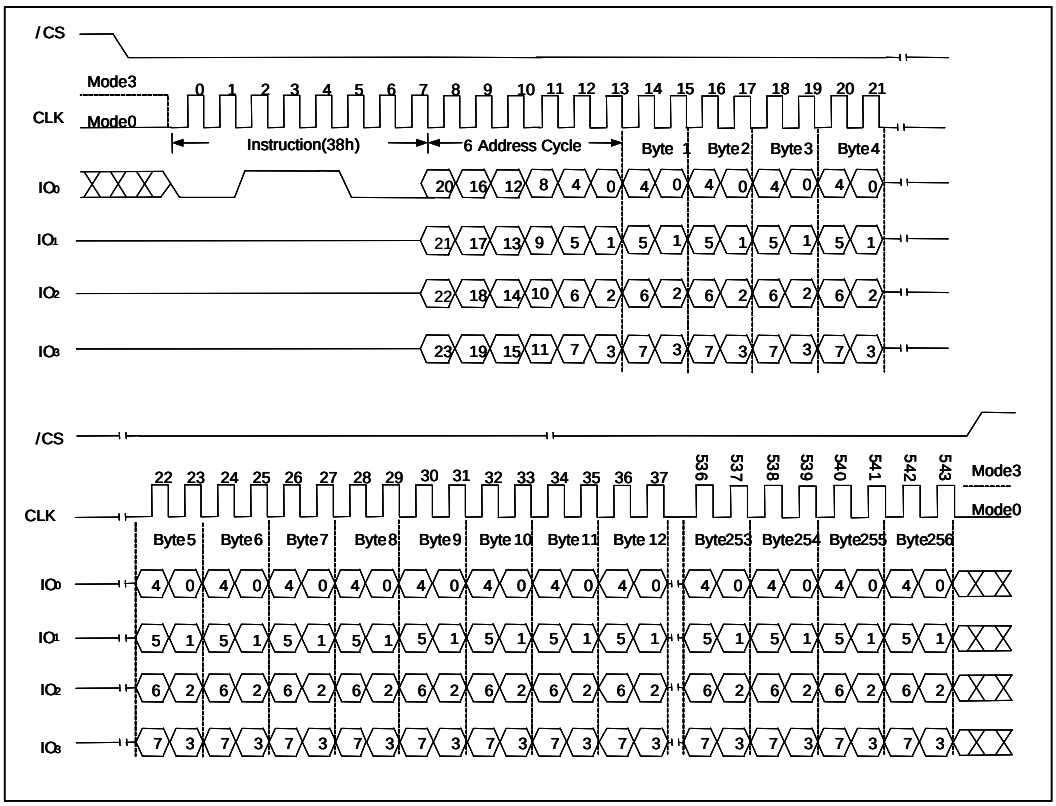



Figure 15. Quad Page Program Instruction Sequence Diagram

### 11.2.16 Sector Erase (20h)

The sector Erase instruction sets all memory within a specified sector (4K-bytes) to the erased state of all 1s (FFh). A Write Enable instruction must be executed before the device will accept the Sector Erase Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the /CS pin low and shifting the instruction code “20h” followed a 24-bit sector address (A23-A0). The Sector Erase instruction sequence is shown in figure 16.

The /CS pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Sector Erase instruction will not be executed. After /CS is driven high, the self-timed Sector Erase instruction will commence for a time duration of tSE (See AC Characteristics). While the Sector Erase cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the Sector Erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Sector Erase cycle has finished the Write Enable Latch (WEL) bit in Status Register is cleared to 0. The Sector Erase instruction will not be executed if the addressed page is protected by the Block Protect (SEC, TB, BP2, BP1, and BP0) bits (see Status Register Memory protection table).

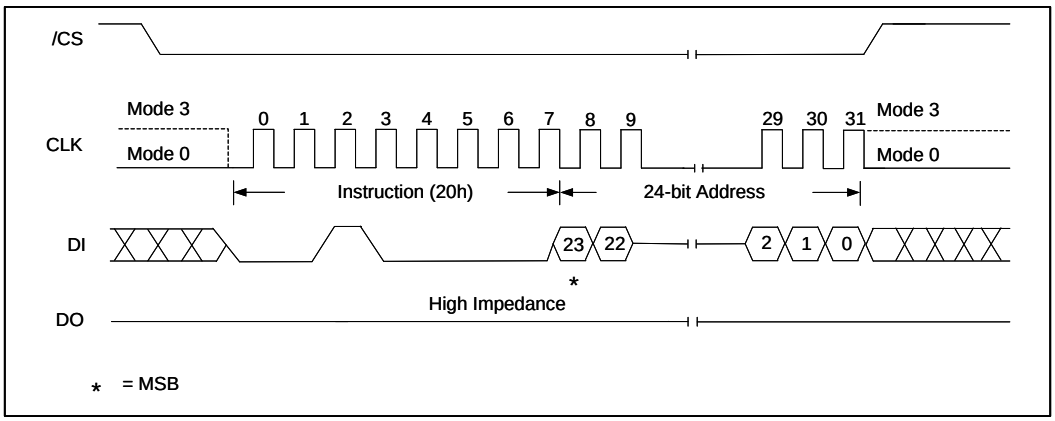



Figure 16. Sector Erase Instruction Sequence Diagram

### 11.2.17 32KB Block Erase (52h)

The Block Erase instruction sets all memory within a specified block (32k-bytes) to the erased state of all 1s (FFh). A Write Enable instruction must be executed before the device will accept the Block Erase Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the /CS pin low and shifting the instruction code “52h” followed a 24-bit block address (A23-A0). The Block Erase instruction sequence is shown in figure 17.

The /CS pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Block Erase instruction will not be executed. After /CS is driven high, the self-timed Block Erase instruction will commence for a time duration of tBE1 (See AC Characteristics). While the Block Erase cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the Block Erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again.
After the Sector Erase cycle has finished the Write Enable Latch (WEL) bit in Status Register is cleared to 0.The Block Erase instruction will not be executed if the addressed page is protected by the Block Protect (SEC, TB, BP2, BP1, and BP0) bits (see Status Register Memory Protection table).

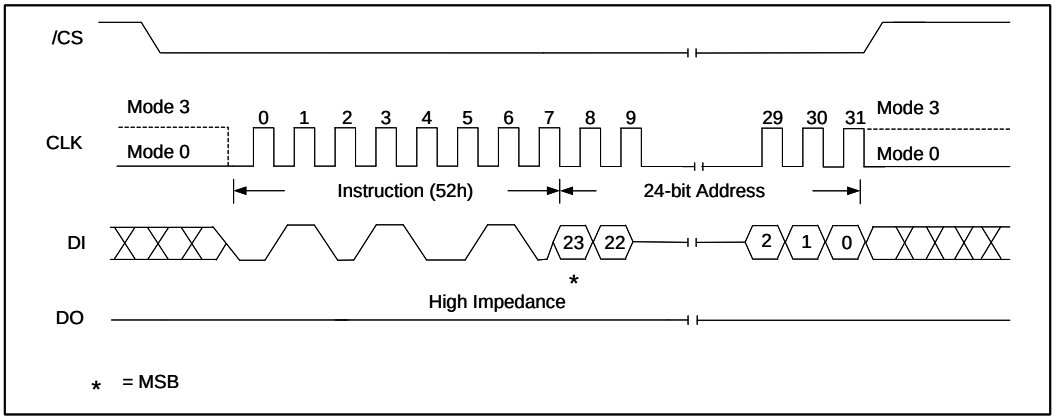



Figure 17. 32KB Block Erase Instruction Sequence Diagram

### 11.2.18 64KB Block Erase (D8h)

The Block Erase instruction sets all memory within a specified block (64k-bytes) to the erased state of all 1s (FFh). A Write Enable instruction must be executed before the device will accept the Block Erase Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the /CS pin low and shifting the instruction code "D8h" followed a 24-bit block address (A23-A0). The Block Erase instruction sequence is shown in figure 18.

The /CS pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Block Erase instruction will not be executed. After /CS is driven high, the self-timed Block Erase instruction will commence for a time duration of tBE1 (See AC Characteristics). While the Block Erase cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the Block Erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Block Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Block Erase instruction will not be executed if the addressed page is protected by the Block Protect (SEC, TB, BP2, BP1, and BP0) bits (see Status Register Memory Protection table).

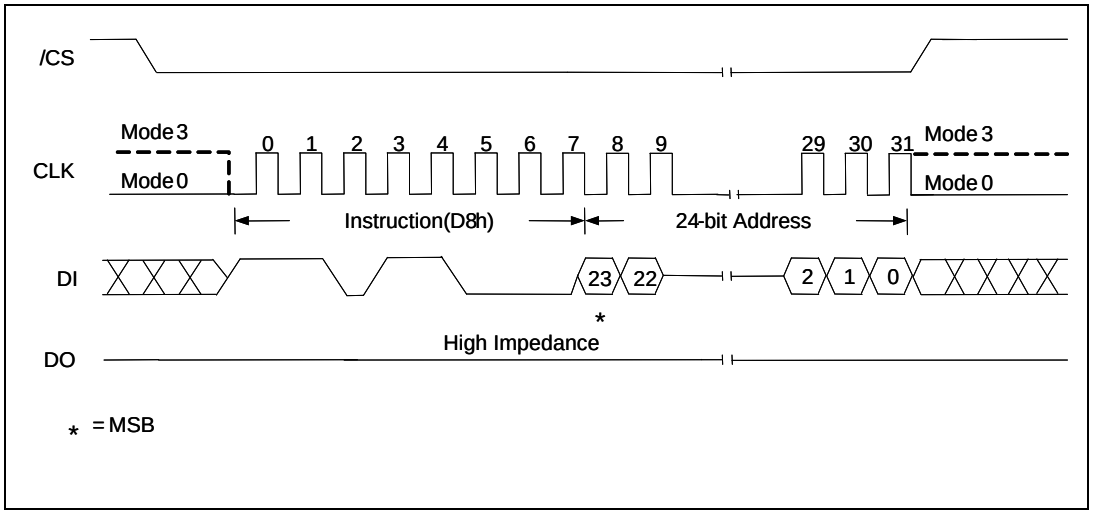



Figure 18. 64KB Block Erase Instruction Sequence Diagram

### 11.2.19 Chip Erase (C7h / 60h)

The Chip Erase instruction sets all memory within the device to the erased sate of all 1s (FFh). A Write Enable instruction must be executed before the device will accept the Chip Erase Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the /CS pin low and shifting the instruction code “C7h” or “60h”. The Chip Erase instruction sequence is shown in figure 19.

The /CS pin must be driven high after the eighth bit has been latched. If this is not done the Chip Erase instruction will not be executed. After /CS is driven high, the self-timed Chip Erase instruction will commence for a time duration of tCE (See AC Characteristics). While the Chip Erase cycle is in progress, the Read Status Register instruction may still be accessed to check the status of the BUSY bit. The BUSY bit is a 1 during the Chip Erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Chip Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Chip Erase instruction will not be executed if any page is protected by the Block Protect (SEC, TB, BP2, BP1, and BP0) bits (see Status Register Memory Protection table).

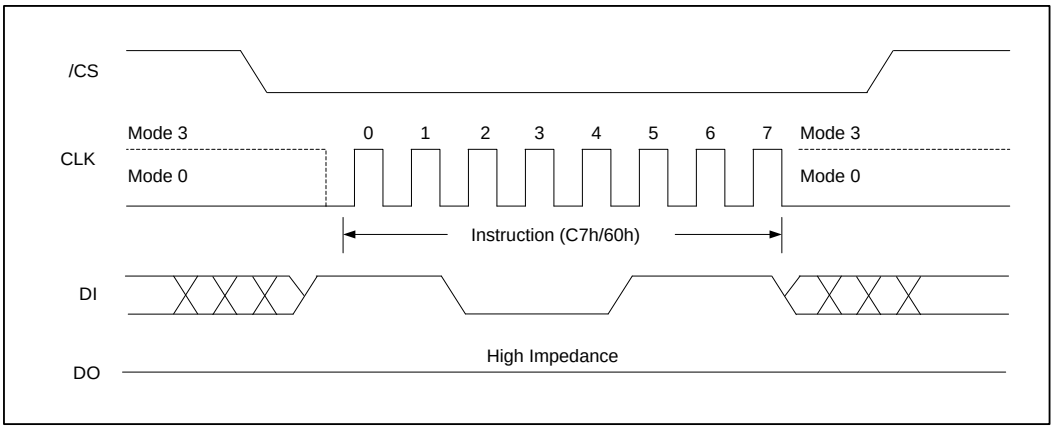



Figure 19. Chip Erase Instruction Sequence Diagram

### 11.2.20 Erase / Program Suspend (75h)

The Erase/Program Suspend instruction “75h”, allows the system to interrupt a Sector or Block Erase operation or a Page Program operation and then read from or program data to, any other sectors or blocks. The Erase/Program Suspend instruction sequence is shown in figure 20.

The Write Status Register instruction (01h) and Erase instructions (20h, 52h, D8h, C7h, 60h) are not allowed during Erase Suspend. Erase Suspend is valid only during the Sector or Block erase operation. If written during the Chip Erase operation, the Erase Suspend instruction is ignored. The Write Status Register instruction (01h) and Program instructions (02h, 32h, 38h) are not allowed during Program Suspend. Program Suspend is valid only during the Page Program or Quad Page Program operation.

The Erase/Program Suspend instruction “75h” will be accepted by the device only if the SUS bit in the Status Register equals to 0 and the BUSY bit equals to 1 while a Sector or Block Erase or a Page Program operation is on-going. If the SUS bit equals to 1 or the BUSY bit equals to 0, the Suspend instruction will be ignored by the device. A maximum of time of “tSUS” (See AC Characteristics) is required to suspend the erase or program operation. The BUSY bit in the Status Register will be cleared from 1 to 0 within “tSUS” and the SUS bit in the Status Register will be set from 0 to 1 immediately after Erase/Program Suspend. For a previously resumed Erase/Program operation, it is also required that the Suspend instruction “75h” is not issued earlier than a minimum of time of “tSUS” following the preceding Resume instruction “7Ah”.

Unexpected power off during the Erase/Program suspend state will reset the device and release the suspend state. SUS bit in the Status Register will also reset to 0. The data within the page, sector or block that was being suspended may become corrupted. It is recommended for the user to implement system design techniques against the accidental power interruption and preserve data integrity during erase/program suspend state.

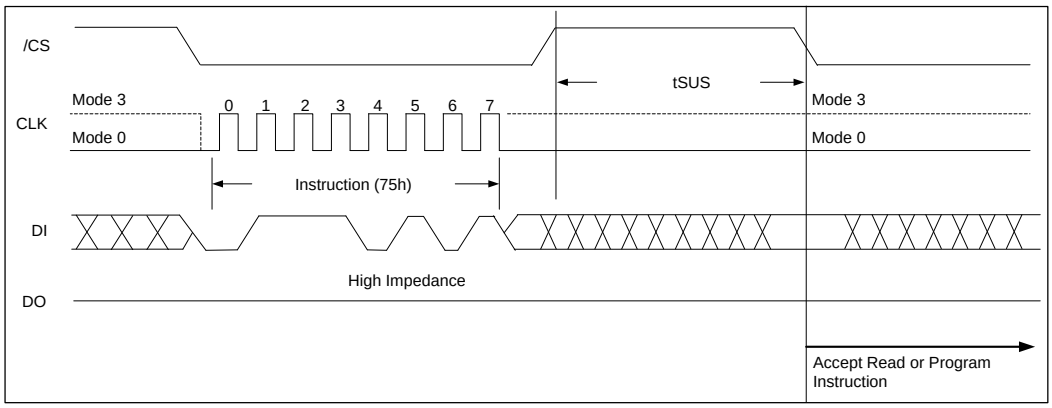



Figure 20. Erase Suspend instruction Sequence

### 11.2.20 Erase / Program Resume (7Ah)

The Erase/Program Resume instruction “7Ah” must be written to resume the Sector or Block Erase operation or the Page Program operation after an Erase/Program Suspend. The Resume instruction “7Ah” will be accepted by the device only if the SUS bit in the Status Register equals to 1 and the BUSY bit equals to 0. After issued the SUS bit will be cleared from 1 to 0 immediately, the BUSY bit will be set from 0 to 1 within 200ns and the Sector or Block will complete the erase operation or the page will complete the program operation. If the SUS bit equals to 0 or the BUSY bit equals to 1, the Resume instruction “7Ah” will be ignored by the device. The Erase/Program Resume instruction sequence is shown in figure 20.

Resume instruction is ignored if the previous Erase/Program Suspend operation was interrupted by unexpected power off. It is also required that a subsequent Erase/Program Suspend instruction not to be issued within a minimum of time of “t SUS ” following a previous Resume instruction.

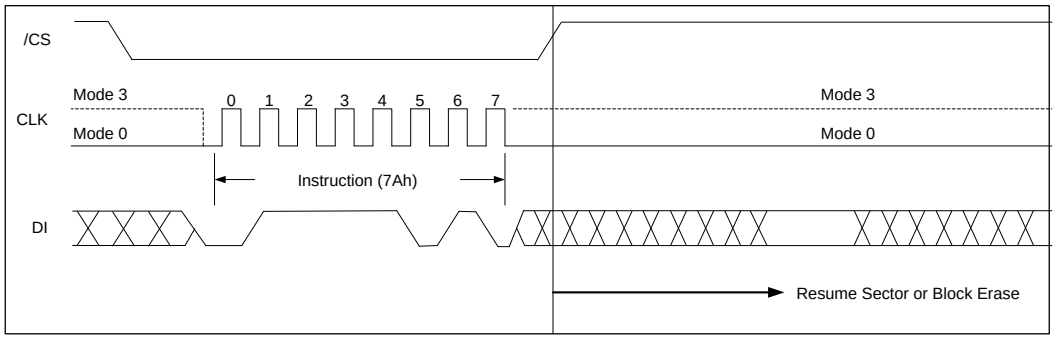



Figure 20. Erase / Program Resume instruction Sequence

### 11.2.22 Power-down (B9h)

Although the standby current during normal operation is relatively low, standby current can be further reduced with the Power-down instruction. The lower power consumption makes the Power-down instruction especially useful for battery powered applications (See ICC1 and ICC2 in AC Characteristics). The instruction is initiated by driving the /CS pin low and shifting the instruction code “B9h” as shown in figure 22.

The /CS pin must be driven high after the eighth bit has been latched, If this is not done the Power-down instruction will not be executed. After /CS is driven high, the Power-down state will be entered within the time duration of tDP (See AC Characteristics). While in the Release power-down /Device ID instruction, which restores the device to normal operation, will be recognized. All other instructions are ignored. This includes the Read Status Register instruction, which is always available during normal operation. Ignoring all but one instruction makes the Power Down state a useful condition for securing maximum write protection. The device always powers-up in the normal operation with the standby current of ICC1.

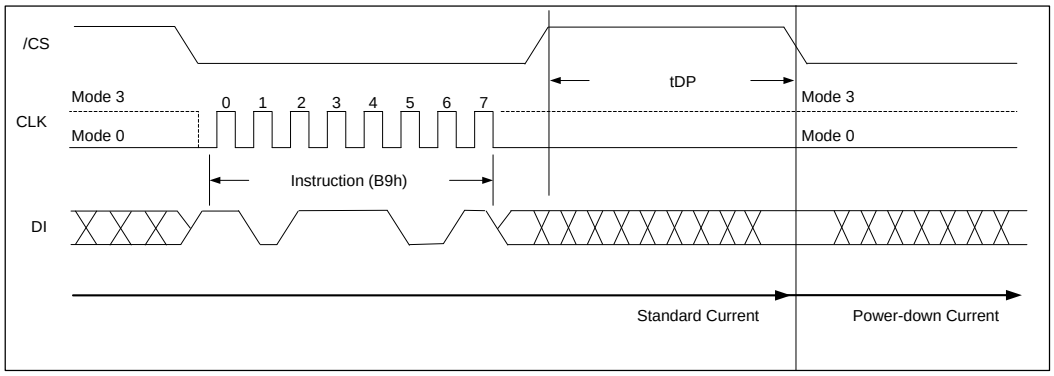



Figure 22. Deep Pwer-down Instruction Sequence Diagram

### 11.2.23 Release Power-down / Device ID (ABh)

The Release from Power-down / Device ID instruction is a multi-purpose instruction. It can be used to release the device from the power-down state or obtain the device electronic identification (ID) number.

To release the device from the power-down state, the instruction is issued by driving the /CS pin low, shifting the instruction code “ABh” and driving /CS high as shown in figure 23a. Release from power-down will take the time duration of tRES1 (See AC Characteristics) before the device will resume normal operation and other instructions are accepted. The /CS pin must remain high during the tRES1 time duration.

When used only to obtain the Device ID while not in the power-down state, instruction is initiated by driving the /CS pin low and shifting the instruction code “ABh” followed by 3-dummy bytes. The Device ID bits are then shifted on the falling edge of CLK with most significant bit (MSB) first as shown in figure 23b. The Device ID value for the FM25Q32 is listed in Manufacturer and Device Identification table. The Device ID can be read continuously. The instruction is completed by driving /CS high.

When used to release the device from the power-down state and obtain the Device ID, the

instruction is the same as previously described, and shown in figure 23b, except that after /CS is driven high it must remain high for a time duration of tRES2 (See AC Characteristics). After this time duration the device will resume normal operation and other instructions will be accepted. If the Release from power-down /Device ID instruction is issued while an Erase, Program or Write cycle is in process (when BUSY equals 1) the instruction is ignored and will not have any effects on the current cycle.

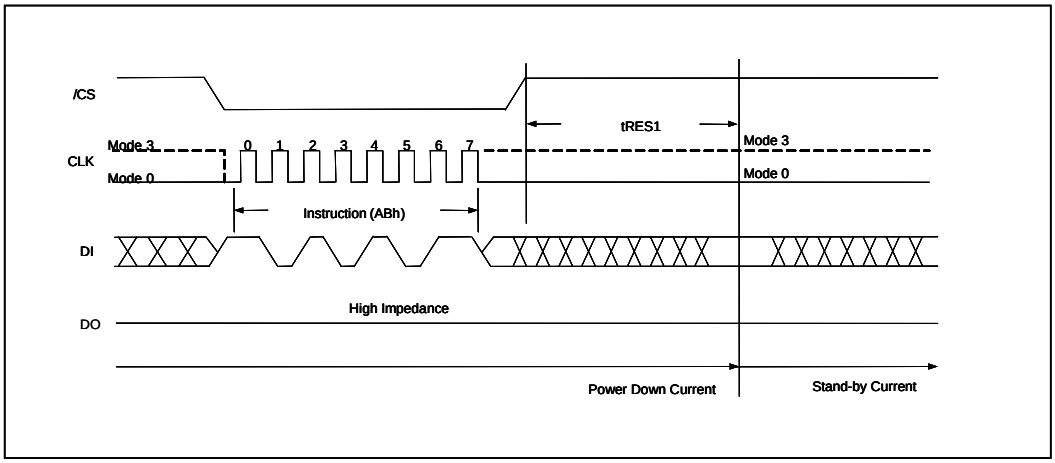



Figure 23a. Release power-down Instruction Sequence

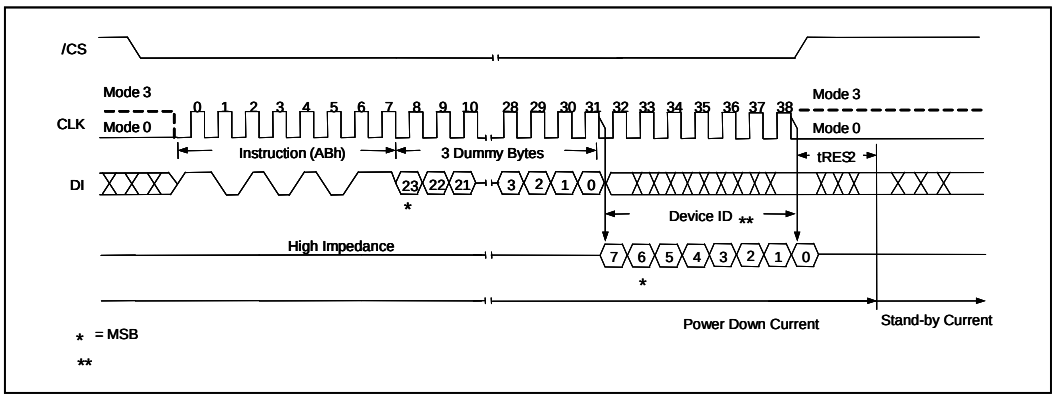



Figure 23b. Release power-down / Device ID Instruction Sequence Diagram

### 11.2.24 Read Manufacturer/ Device ID (90h),(EFh),(DFh)

The Read Manufacturer/ Device ID instruction is an alternative to the Release from Power-down / Device ID instruction that provides both the JEDEC assigned manufacturer ID and the specific device ID.

The Read Manufacturer/ Device ID instruction is very similar to the Release from Power-down / Device ID instruction. The instruction is initiated by driving the /CS pin low and shifting the instruction code “90h” or “EFh” or “DFh” followed by a 24-bit address (A23-A0) of 000000h. After which, the Manufacturer ID for FIDELIX SEMICONDUCTOR (F8h) and the Device ID are shifted out on the falling edge of CLK with most significant bit(MSB) first as shown in figure 24a, 24b or 24c. The Device ID value for the FM25Q32 is listed in Manufacturer and Device Identification table. If the 24-bit address is initially set to 000001h the Device ID will be read first and then followed by the Manufacturer ID. The Manufacturer and Device IDs can be read continuously, alternating from one to the other. The instruction is completed by driving/CS high.

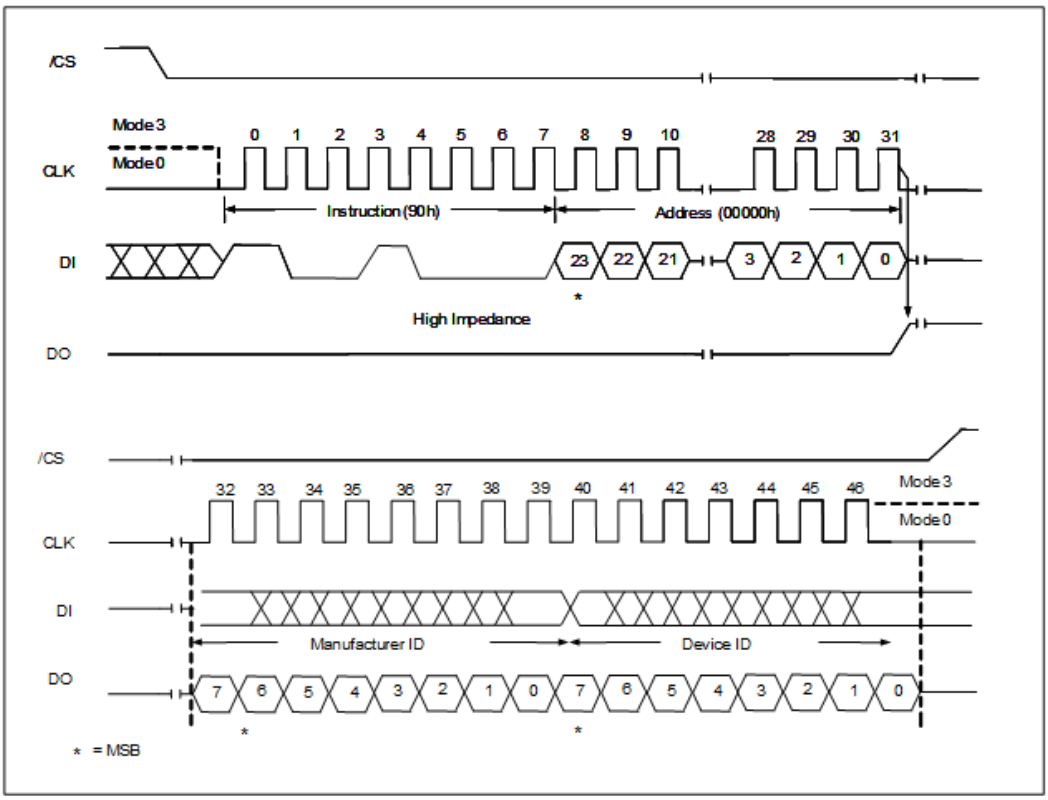



Figure 24a. Read Manufacturer/ Device ID Diagram

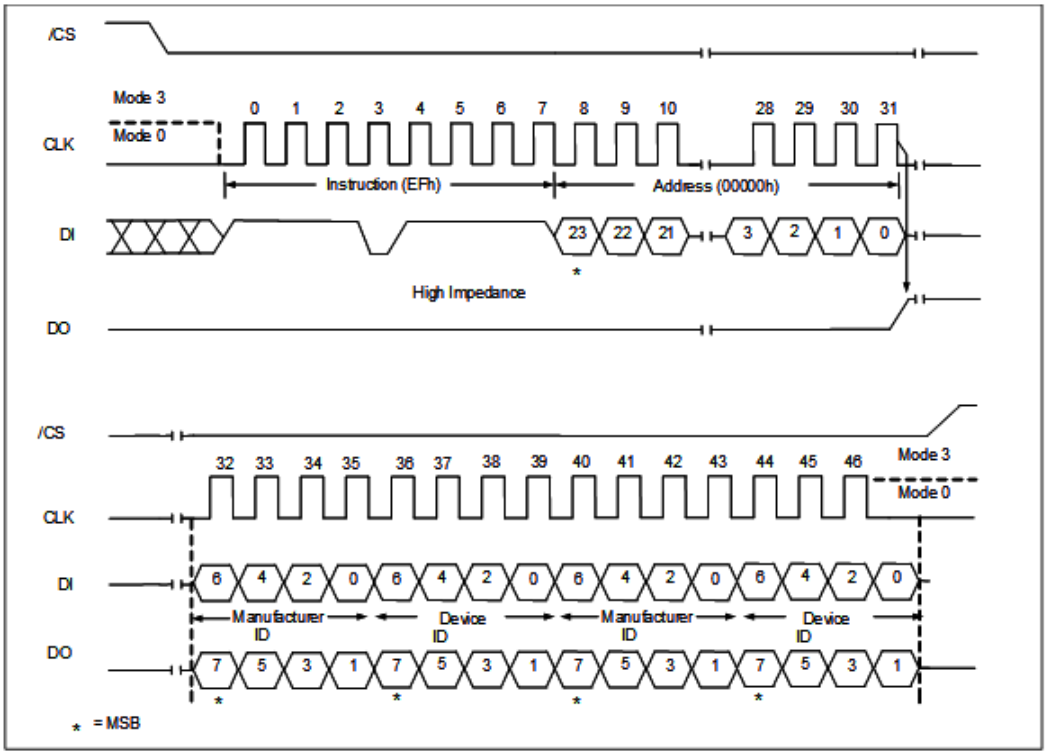



Figure 23b. Read Dual Manufacturer/ Device ID Diagram

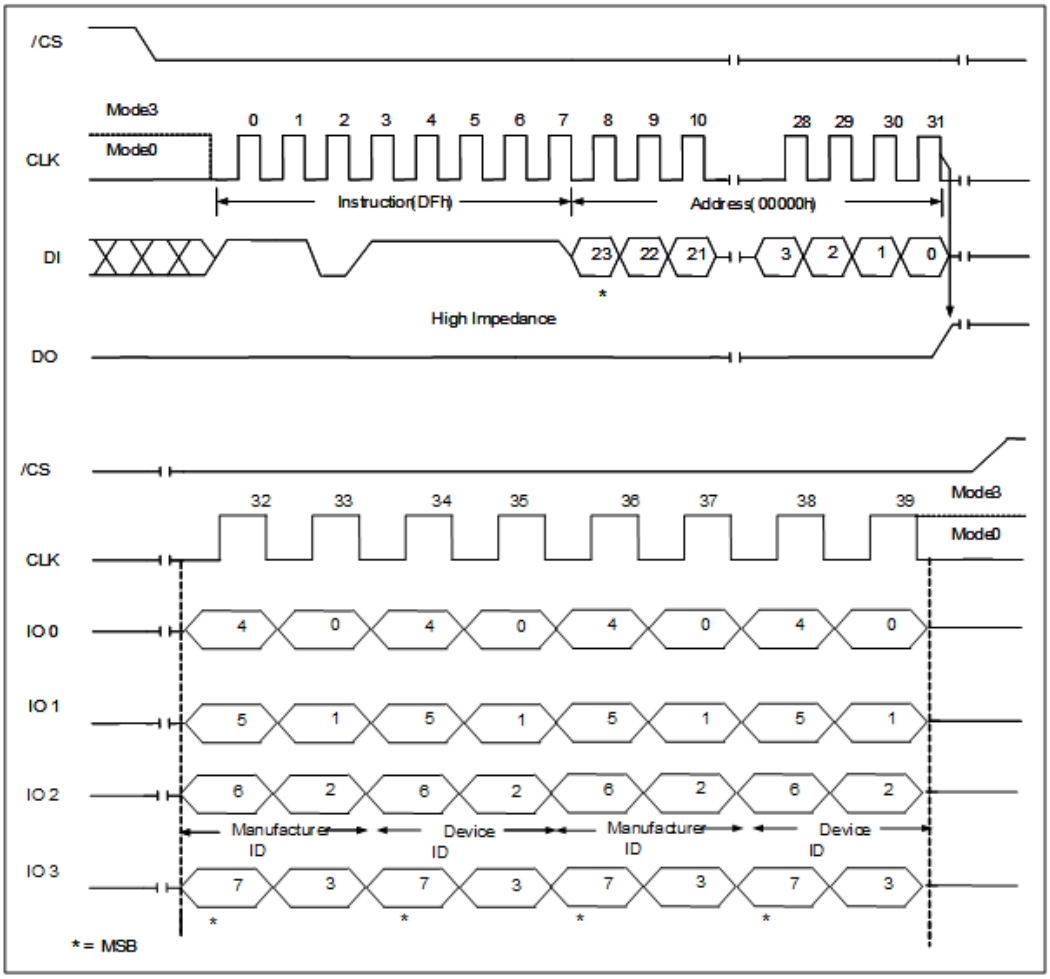



Figure 23c. Read Quad Manufacturer/ Device ID Diagram

### 11.2.25 JEDEC ID (9Fh)

For compatibility reasons, the FM25Q32 provides several instructions to electronically determine the identity of the device. The Read JEDEC ID instruction is compatible with the JEDEC standard for SPI compatible serial memories that was adopted in 2003. The instruction is initiated by driving the /CS pin low and shifting the instruction code "9Fh". The instruction JEDEC assigned Manufacturer ID byte for FIDELIX SEMICONDUCTOR(F8h) and two Device ID bytes, Memory Type(ID-15-ID8) and Capacity (ID7-ID0) are then shifted out on the falling edge of CLK with most significant bit (MSB) first shown in figure 25. For memory type and capacity values refer to Manufacturer and Device Identification table. The JEDEC ID can be read continuously. The instruction is completed by driving/CS high.

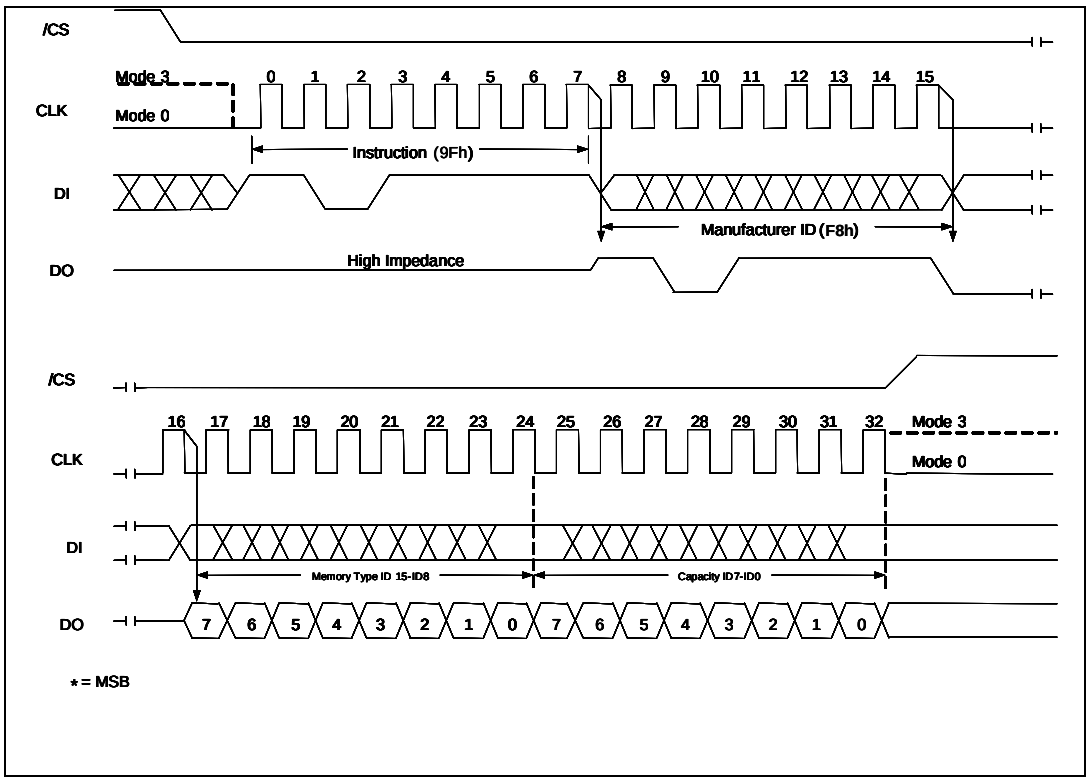



Figure 25. Read JEDEC ID

### 11.2.26 Mode Bit Reset (FFh)

For Fast Read Dual/Quad I/O operations, Mode Bits (M7-0) are implemented to further reduce instruction overhead. By setting the Mode Bits (M7-0) to “Ax” hex, the next Fast Read Dual/Quad I/O operations do not require the BBh/EBh instruction code (See 11.2.10 Fast Read Dual I/O and 11.2.11 Fast Read Quad I/O for detail descriptions).

If the system controller is reset during operation it will likely send a standard SPI instruction, such as Read ID (9Fh) or Fast Read (0Bh), to the FM25Q32. However, as with most SPI Serial Flash memories, the FM25Q32 does not have a hardware Reset pin, so if Mode bits are set to “Ax” hex, the FM25Q32 will not recognize any standard SPI instruction. To address this possibility, it is recommended to issue a Mode Bit Reset instruction “FFh” as the first instruction after a system Reset. Doing so will release the mode Bits for the “Ax” hex state and allow Standard SPI instruction to be recognized. The Mode Bits Reset instruction is shown in figure 26.

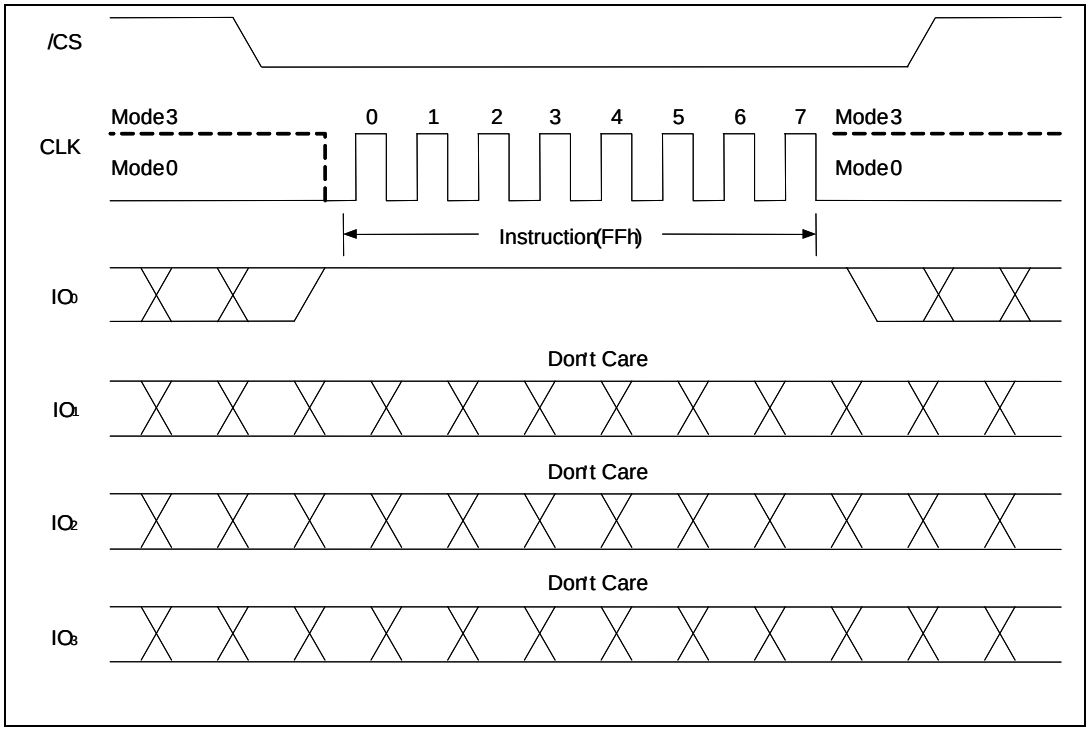



Figure 26. Mode Bits Reset for Fast Read Dual/Quad I/O

### 11.2.27 Enter Secured OTP (B1h)

The Enter Secured OTP instruction is for entering the additional 4K-bit secured OTP mode. The additional 4K-bit secured OTP is independent from main array, which may be used to store unique serial number for system identifier. After entering the Secured OTP mode, and then follow standard read or program, procedure to read out the data or update data. The Secured OTP data cannot be updated again once it is lock-down

Please note that WRSR/WRSCUR commands are not acceptable during the access of secure OTP region, once security OTP is lock down, only commands related with read are valid.
The Enter Secured OTP instruction sequence is shown in figure 27.

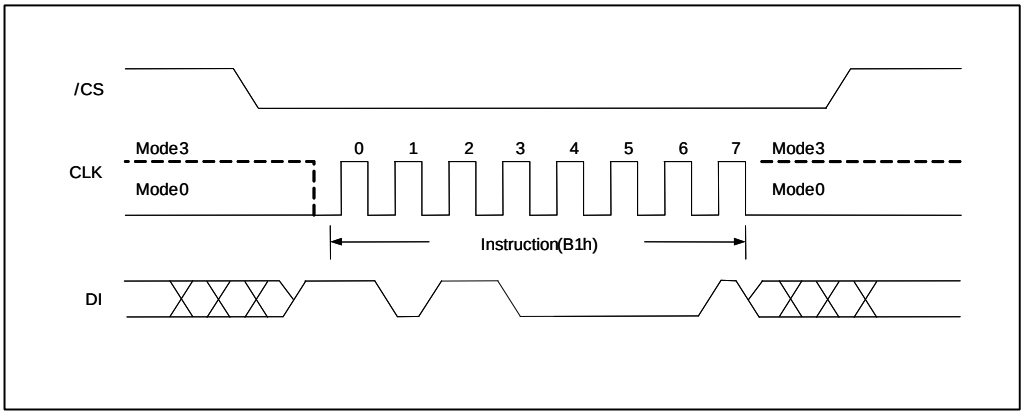



Figure 27. Enter Secured OTP instruction sequence

### 11.2.28 Exit Secured OTP (C1h)

The Exit Secured OTP instruction is for exiting the additional 4K-bit secured OTP mode.
The Exit Secured OTP instruction sequence is shown in figure 28

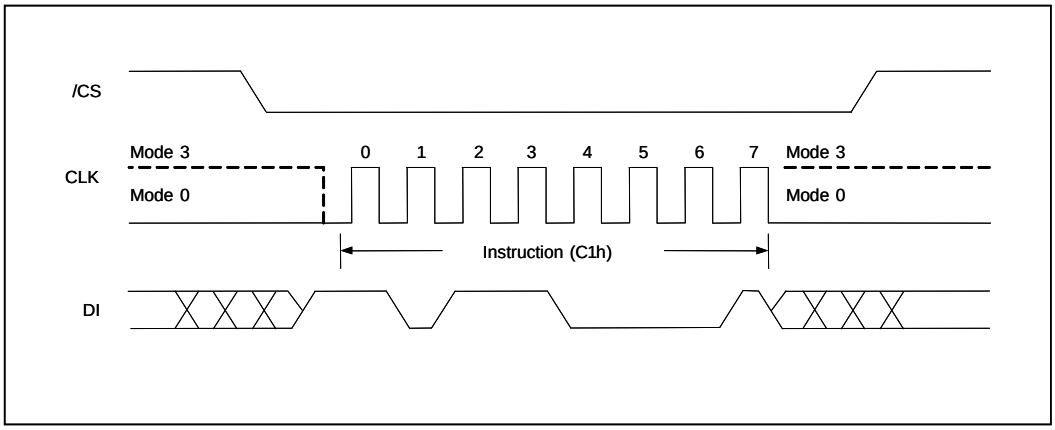



Figure 28. Exit Secured OTP instruction sequence

### 11.2.29 Read Security Register (2Bh)

The Read Security Register instruction is for reading the value of Security Register bits. The Read Security Register can be read at any time (even in program/erase/write status register condition) and continuously.

The definition of the Security Register bits is as below:

**Secured OTP Indicator bit.** The Secured OTP indicator bit shows the chip is locked by factory before ex-factory or not. When it is “0”, it indicates non-factory lock, “1” indicates factory-lock.

**Lock-down Secured OTP (LDSO) bit.** By writing WRSCUR instruction, the LDSO bit may be set to “1” for customer lock-down purpose. However, once the bit it set to “1” (Lock-down), the LDSO bit and the 4K-bit Secured OTP area cannot be updated any more. While it is in 4K-bit Secured OTP mode, array access is not allowed to write.

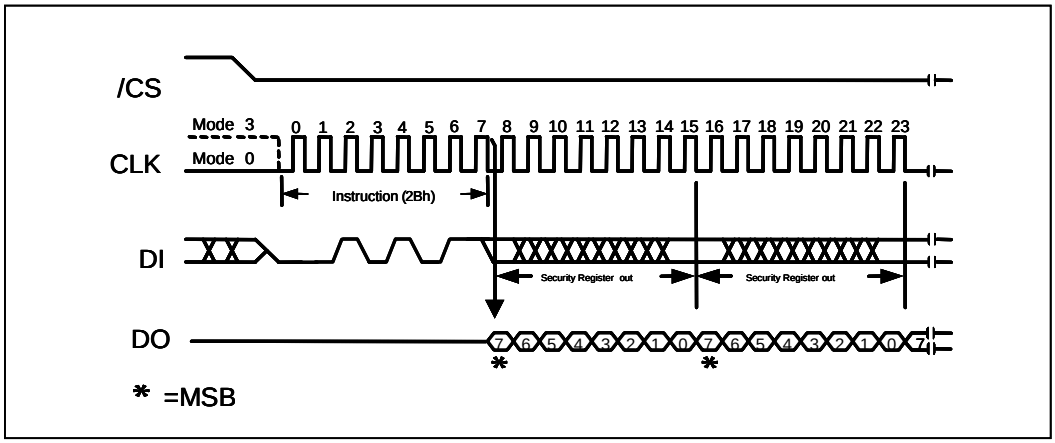



Figure 29. Read Security Register instruction sequence

**Security Register Definition**

| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---|---|---|---|---|---|---|---|
| x | x | x | x | x | x | LDSO (indicate if lock-down) | Secured OTP indicator bit |
| reserved | reserved | reserved | reserved | reserved | reserved | 0 = not lock-down<br>1 = lock-down(cannot program/erase OTP) | 0 = non factory lock<br>1 = factory lock |
| Volatile bit | Volatile bit | Volatile bit | Volatile bit | Volatile bit | Volatile bit | Non-Volatile bit | Non-Volatile bit |

### 11.2.30 Write Security Register (2Fh)

The Write Security Register instruction is for changing the values of Security Register bits. Unlike Write Status Register, the WREN instruction is not required before writing WRSCUR instruction. The WRSCUR instruction may change the value of bit1 (LDSO bit) for customer to lock-down the 4K-bit Secured OTP area. Once the LDSO bit is set to “1”, the Secured OTP area cannot be updated any more.

The /CS must go high exactly at the boundary; otherwise, the instruction will be rejected and not executed.

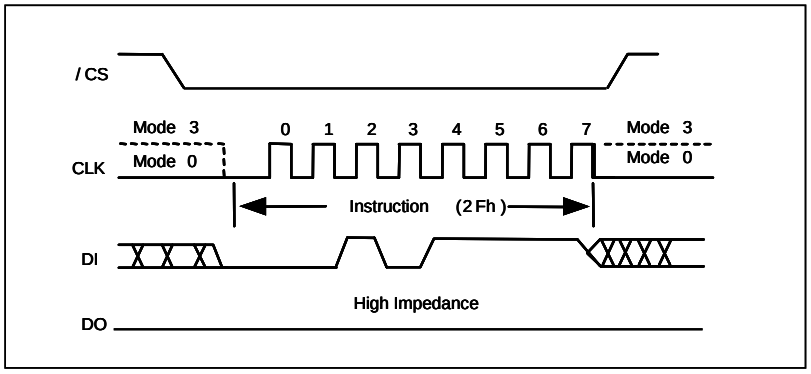



Figure 30. Write Security Register instruction sequence

### 11.2.31 4K-bit Secured OTP

It’s for unique identifier to provide 4K-bit one-time-program area for setting device unique serial number which may be set by factory or system customer. Please refer to table of “4K-bit secured OTP definition”.

- Security register bit 0 indicates whether the chip is locked by factory or not.
- To program the 4K-bit secured OTP by entering 4K-bit secured OTP mode (with ENSO command) and going through normal program procedure, and then exiting 4K-bit secured OTP mode by writing EXSO command
- Customer may lock-down bit1 as “1”. Please refer to “table of security register definition” for security register bit definition and table of “4K-bit secured OTP definition” for address range definition.
- Note. Once lock-down whatever by factory or customer, it cannot be changed any more. While in 4K-bit secured OTP mode, array access is not allowed to write.

**4K-bit secured OTP definition**

| Address range | Size | Standard Factory Lock | Customer Lock |
|---|---|---|---|
| 000000 ~ 00000F | 128-bit | ESN (Electrical Serial Number) | Determined by customer |
| 000010 ~ 0001FF | 3968-bit | N/A | |

### 11.2.32 Set Burst with Wrap (77h)

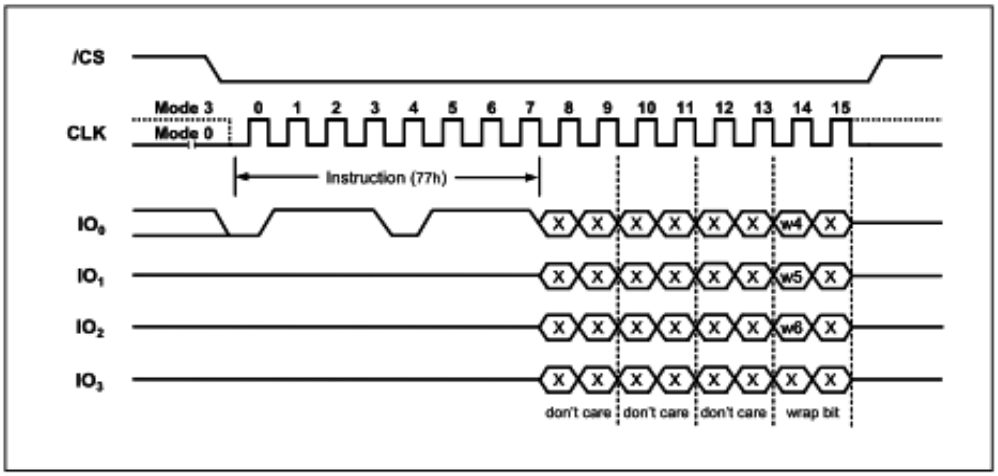
The Set Burst with Wrap (77h) instruction is used in conjunction with "Fast Read Quad I/O" instructions to access a fixed length of 8/16/32/64-byte section within a 256-byte page. Certain applications can benefit from this feature and improve the overall system code execution performance.

Similar to a Quad I/O instruction, the Set Burst with Wrap instruction is initiated by driving the /CS pin low and then shifting the instruction code "77h" followed by 24 dummy bits and 8 "Wrap Bits", W7-0. The instruction sequence is shown in Set Burst with Wrap Instruction Sequence.

Wrap bit W7 and the lower nibble W3-0 are not used.

| W6, W5 | W4 = 0 | | W4 = 1(Default) | |
|---|---|---|---|---|
| | Wrap Around | Wrap Length | Wrap Around | Wrap Length |
| 0 0 | Yes | 8-byte | No | N/A |
| 0 1 | Yes | 16-byte | No | N/A |
| 1 0 | Yes | 32-byte | No | N/A |
| 1 1 | Yes | 64-byte | No | N/A |

Once W6-4 is set by a Set Burst with Wrap instruction, all the following "Fast Read Quad I/O" and instructions will use the W6-4 setting to access the 8/16/32/64-byte section within any page. To exit the "Wrap Around" function and return to normal read operation, another Set Burst with Wrap instruction should be issued to set W4 = 1. The default value of W4 upon power on is 1. In the case of a system Reset while W4 = 0, it is recommended that the controller issues a Set Burst with Wrap instruction to reset W4 = 1 prior to any normal Read instructions since FM25Q32 does not have a hardware Reset Pin.




Set Burst with Wrap Instruction Sequence

# 12. ELECTRICAL CHARACTERISTICS

## 12.1 Absolute Maximum Ratings [1]

| PARAMETERS | SYMBOL | CONDITIONS | RANGE | UNIT |
|---|---|---|---|---|
| Supply Voltage | VCC | | -0.6 to +4.0 | V |
| Voltage Applied to Any Pin | VIO | Relative to Ground | -0.6 to VCC +0.4 | V |
| Transient Voltage on any Pin | VIOT | <20nS Transient Relative to Ground | -2.0V to VCC +2.0V | V |
| Storage Temperature | TSTG | | -65 to +150 | ˚C |
| Lead Temperature | TLEAD | | See Note[3] | ˚C |
| Electrostatic Discharge Voltage | VESD | Human Body Model[4] | -2000 to +2000 | V |

**Notes:**

1. Specification for FM25Q32 is preliminary. See preliminary designation at the end of this document.
2. This device has been designed and tested for the specified operation ranges. Proper operation outside of these levels is not guaranteed. Exposure to absolute maximum ratings may affect device reliability. Exposure beyond absolute maximum ratings may cause permanent damage.
3. Compliant with JEDEC Standard J-STD-20C for small body Sn-Pb or Pb-free (Green) assembly and the European directive on restrictions on hazardous substances (RoHS) 2002/95/EU.
4. JEDEC Std JESD22-A114A (C1=100pF, R1=1500 ohms, R2=500 ohms).

## 12.2 Operating Ranges

| PARAMETER | SYMBOL | CONDITIONS | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| Erase/Program Cycles | VCC | FR1 = 85MHz (Single/Dual/Quad SPI)<br>FR2 = 104MHz (Single/Dual/Quad SPI)<br>fR = 50MHz (Read Data 03h) | 2.7<br>3.0<br>2.7 | 3.6 | V |
| Temperature,Operating | Tj | Industrial | -40 | +85 | ˚C |

## 12.3 Endurance and Data Retention

| PARAMETER | CONDITIONS | MIN | MAX | UNIT |
|---|---|---|---|---|
| Erase/Program Cycles | 4KB sector, 32/64KB block or full chip. | 100,000 | | Cycles |
| Data Retention | Full Temperature Range | | 20 | years |

## 12.4 Power-up Timing and Write Inhibit Threshold

| PARAMETER | SYMBOL | SPEC | | UNIT |
|---|---|---|---|---|
| | | MIN | MAX | |
| VCC(min) to /CS Low | tVSL(1) | 10 | | μs |
| Time Delay Before Write Instruction | tPUW(1) | 1 | 10 | ms |
| Write Inhibit Threshold Voltage | VWI(1) | 1 | 2 | V |

**Note:**

1. These parameters are characterized only.

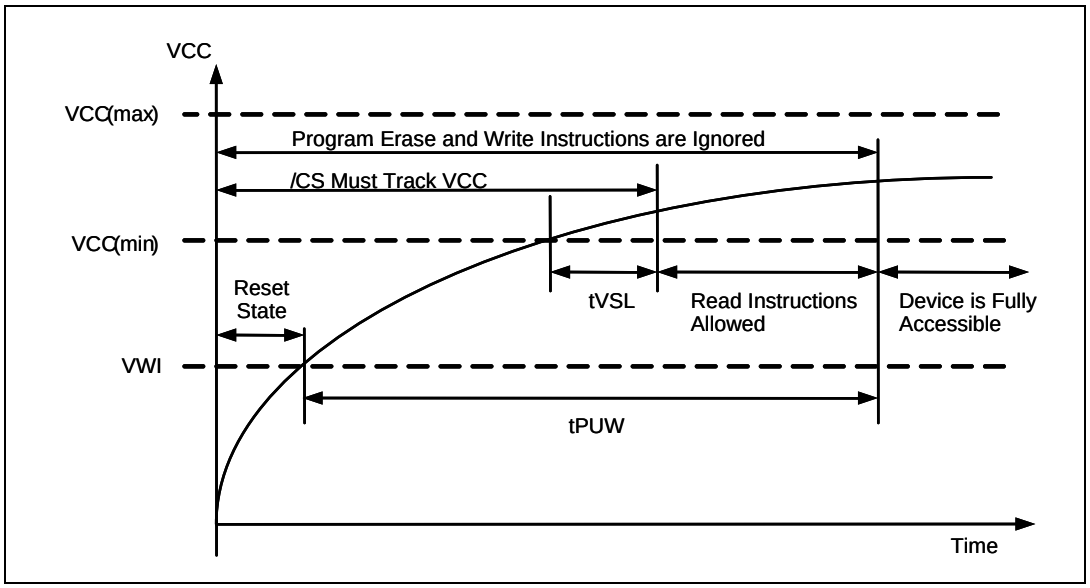



Figure 30. Power-up Timing and Voltage Levels

## 12.5 DC Electrical Characteristics

| PARAMETER | SYMBOL | CONDITION | SPEC | | | UNIT |
|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | |
| Input Capacitance | CIN(1) | VIN=0V(2) | | | 6 | pF |
| Output Capacitance | COUT(1) | VOUT=0V(2) | | | 8 | pF |
| Input Leakage | ILI | | | | ±2 | μA |
| I/O Leakage | ILO | | | | ±2 | μA |
| Standby Current | ICC1 | /CS=VCC, VIN=GND or VCC | | 10 | 50 | μA |
| Power-down Current | ICC2 | /CS=VCC, VIN=GND or VCC | | 1 | 5 | μA |
| Current Read Data/ Dual/Quad 1MHz(2) | ICC3 | C=0.1 VCC / 0.9VCC IO=Open | | 4/5/6 | 6/7.5/9 | mA |
| Current Read Data/ Dual/Quad 33MHz(2) | ICC3 | C=0.1 VCC / 0.9VCC IO=Open | | 6/7/8 | 9/10.5/12 | mA |
| Current Read Data/ Dual/Quad 50MHz(2) | ICC3 | C=0.1 VCC / 0.9VCC IO=Open | | 7/8/9 | 10/12/13.5 | mA |
| Current Read Data/ Dual/Quad 85MHz(2) | ICC3 | C=0.1 VCC / 0.9VCC IO=Open | | 10/11/12 | 15/16.5/18 | mA |
| Current Write Status Register | ICC4 | /CS=VCC | | 8 | 12 | mA |
| Current page Program | ICC5 | /CS=VCC | | 20 | 25 | mA |
| Current Sector/Block Erase | ICC6 | /CS=VCC | | 20 | 25 | mA |
| Current Chip Erase | ICC7 | /CS=VCC | | 20 | 25 | mA |
| Input Low Voltages | VIL | | -0.5 | | VCC x0.2 | V |
| Input High Voltages | VIH | | VCC x0.8 | | VCC +0.4 | V |
| Output Low Voltages | VOL | IOL=1.6mA | | | 0.4 | V |
| Output High Voltages | VOH | IOH=-100μA | VCC -0.2 | | | V |

**Notes:**

1. Tested on sample basis and specified through design and characterization data, TA = 25˚C, VCC = 3V.
2. Checked Board Pattern.

## 12.6 AC Measurement Conditions

| PARAMETER | SYMBOL | SPEC | | UNIT |
|---|---|---|---|---|
| | | MIN | MAX | |
| Load Capacitance | $C_L$ | | 30 | pF |
| Input Rise and Fall Times | $T_R$, $T_F$ | | 5 | ns |
| Input Pulse Voltages | $V_{IN}$ | 0.2 VCC to O. 8 VCC | | V |
| Input Timing Reference Voltages | IN | 0.3 VCC to O. 7 VCC | | V |
| Output Timing Reference Voltages | OUT | 0.5 VCC to O. 5 VCC | | V |

**Note:**

1. Output Hi-Z is defined as the point where data out is no longer driven.

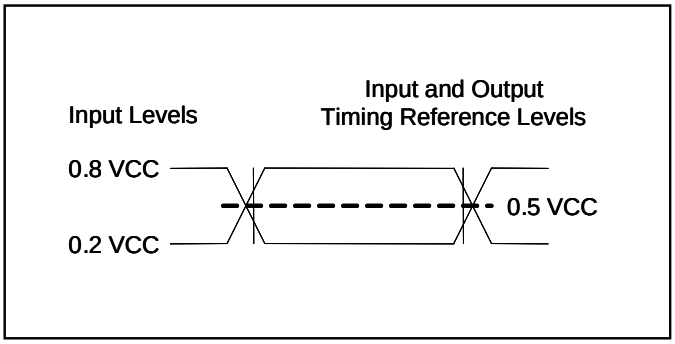



Figure 31. AC Measurement I/O Waveform

## 12.7 AC Electrical Characteristics

| DESCRIPTION | SYMBOL | ALT | SPEC | | | UNIT |
|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | |
| Clock frequency<br>For all instructions, except Read Data (03h)<br>2.7V-3.6V VCC & Industrial Temperature | FR1 | $f_c$ | D.C. | | 85 | MHz |
| Clock frequency<br>For all instructions, except Read Data (03h)<br>3.0V-3.6V VCC & Commercial Temperature | FR2 | $f_c$ | D.C. | | 104 | MHz |
| Clock freq. Read Data instruction (03h) | $f_R$ | | D.C. | | 50 | MHz |
| Clock High, Low Time except Read Data (03h) | tCLH,<br>tCLL(1) | | 4 | | | ns |
| Clock High, Low Time for Read Data (03h) instructions | tCRLH,<br>tCRLL(1) | | 6 | | | ns |
| Clock Rise Time peak to peak | tCLCH(2) | | 0.1 | | | V/ns |
| Clock Fall Time peak to peak | tCHCL(2) | | 0.1 | | | V/ns |
| /CS Active Setup Time relative to CLK | tSLCH | tCSS | 7 | | | ns |
| /CS Not Active Hold Time relative to CLK | tCHSL | | 5 | | | ns |
| Data In Setup Time | tDVCH | tDSU | 4 | | | ns |
| Data In Hold Time | tCHDX | tDH | 4 | | | ns |
| /CS Active Hold Time relative to CLK | tCHSH | | 7 | | | ns |
| /CS Not Active Setup Time relative to CLK | tSHCH | | 7 | | | ns |
| /CS Deselect Time (for Read instructions/ Write, Erase and Program instructions) | tSHSL | tCSH | 10/40 | | | ns |
| Output Disable Time | tSHQZ(2) | tDIS | | | 7 | ns |
| Clock Low to Output Valid<br>2.7V-3.6V / 3.0V-3.6V | tCLQV | tV | | | 7/6 | ns |
| Output Hold Time | tCLQX | tHO | 0 | | | ns |
| /Hold Active Setup Time relative to CLK | tHLCH | | 7 | | | ns |

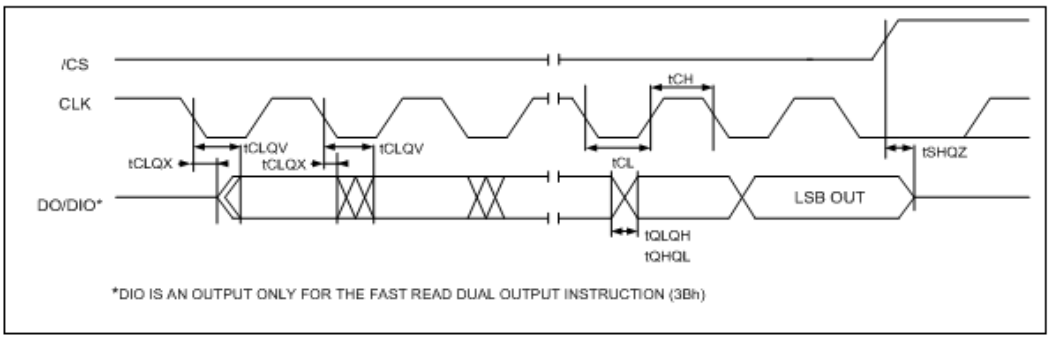
## 12.8 AC Electrical Characteristics (cont'd)

| DESCRIPTION | SYMBOL | ALT | SPEC | | | UNIT |
|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | |
| /HOLD Active Hold Time relative to CLK | tCHHH | | 5 | | | ns |
| /HOLD Not Active Setup Time relative to CLK | tHHCH | | 7 | | | ns |
| /HOLD Not Active Hold Time relative to CLK | tCHHL | | 5 | | | ns |
| /HOLD to Output Low-Z | tHHQX(2) | $t_{LZ}$ | | | 7 | ns |
| /HOLD to Output High-Z | tHLQZ(2) | $t_{HZ}$ | | | 12 | ns |
| Write Protect Setup Time Before /CS Low | tWHSL(3) | | 20 | | | ns |
| Write Protect Setup Time After /CS High | tSHWL(3) | | 100 | | | ns |
| /CS High to Power-down Mode | tDP(2) | | | | 3 | µs |
| /CS High to Standby Mode without Electronic Signature Read | tRES1(2) | | | | 3 | µs |
| /CS High to Standby Mode with Electronic Signature Read | tRES2(2) | | | | 1.8 | µs |
| /CS High to next Instruction after Suspend | tSUS(2) | | | | 20 | µs |
| Write Status Register Time | tw | | | 10 | 15 | ms |
| Byte Program Time | $t_{BP}$ | | | 10 | 150 | µs |
| Page Program Time | $t_{PP}$ | | | 1.5 | 5 | ms |
| Sector Erase Time(4KB) | $t_{SE}$ | | | 40 | 300 | ms |
| Block Erase Time(32KB) | $t_{BE1}$ | | | 200 | 1000 | ms |
| Block Erase Time(64KB) | $t_{BE2}$ | | | 300 | 1500 | ms |
| Chip Erase Time | $t_{CE}$ | | | 10 | 50 | s |

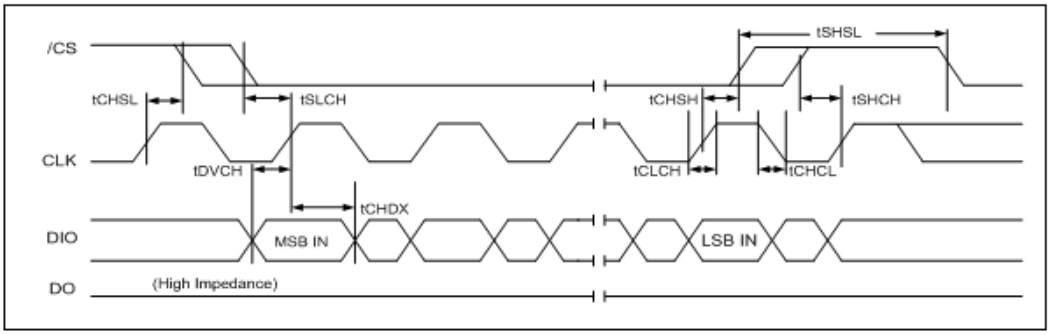
**Notes:**

1. Clock high + Clock low must be less than or equal to 1/fc.
2. Value guaranteed by design and/or characterization, not 100% tested in production.
3. Only applicable as a constraint for a Write Status Register instruction when Sector Protect Bit is set to 1.
4. Commercial temperature only applies to Fast Read ($F_{R1}$ & $F_{R2}$). Industrial temperature applies to all other parameters.

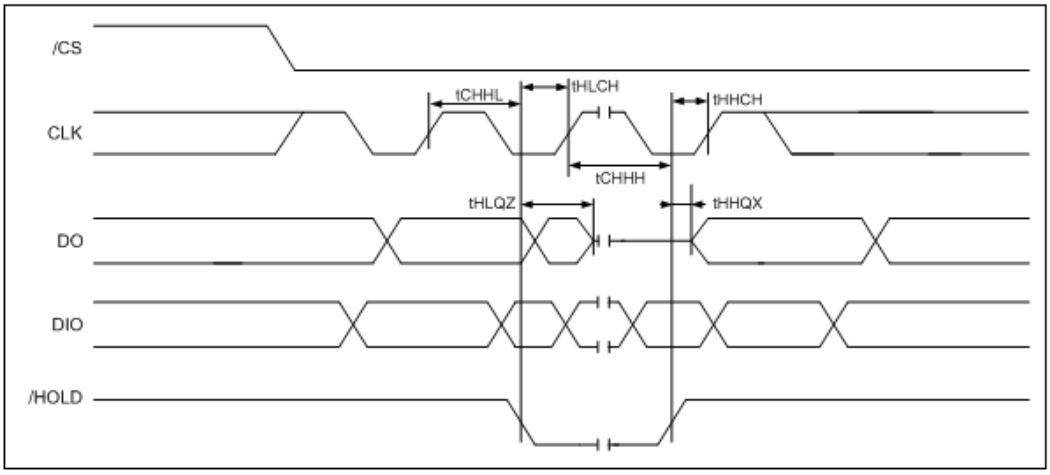
## 12.9 Serial Output Timing




## 12.10 Input Timing

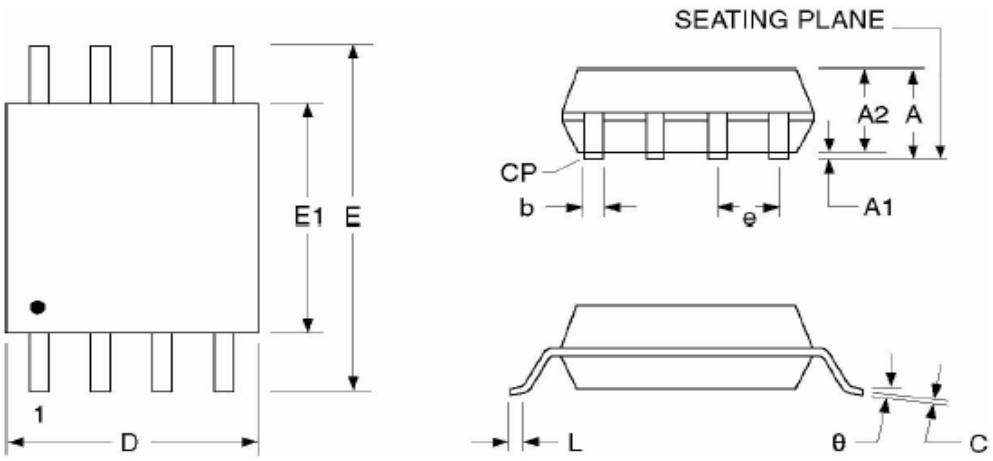



## 12.11 Hold Timing



# 13. PACKAGE SPECIFICATION

## 13.1 8-Pin SOIC 208-mil

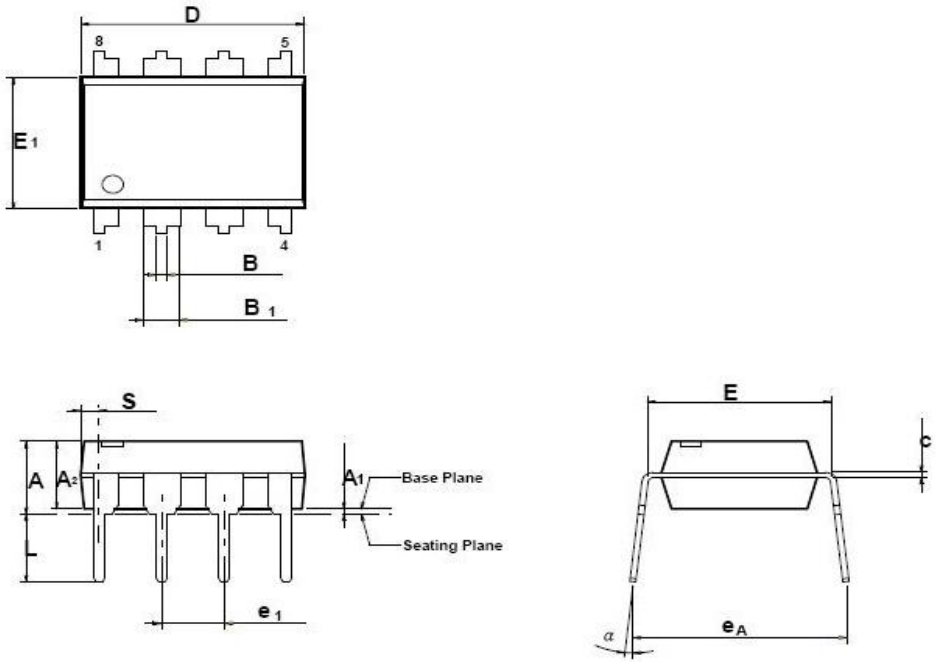



| SYMBOL | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | 1.75 | 2.16 | 0.069 | 0.085 |
| A1 | 0.05 | 0.25 | 0.002 | 0.010 |
| A2 | 1.70 | 1.91 | 0.067 | 0.075 |
| b | 0.35 | 0.48 | 0.014 | 0.019 |
| C | 0.19 | 0.25 | 0.007 | 0.010 |
| D | 5.18 | 5.38 | 0.204 | 0.212 |
| E | 7.70 | 8.10 | 0.303 | 0.319 |
| E1 | 5.18 | 5.38 | 0.204 | 0.212 |
| e | 1.27 BSC | | 0.050 BSC | |
| L | 0.50 | 0.80 | 0.020 | 0.031 |
| θ | 0˚ | 8˚ | 0˚ | 8˚ |
| y | --- | 0.10 | --- | 0.004 |

**Notes:**

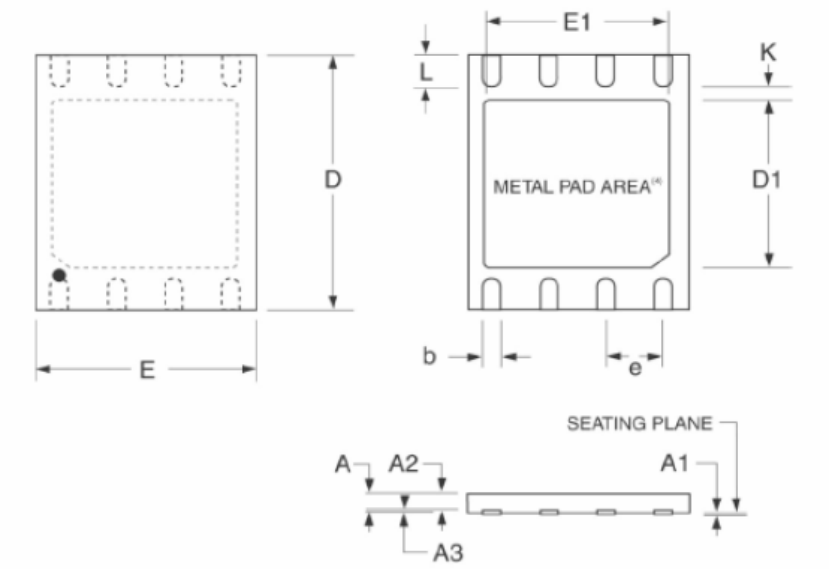
1. Controlling dimensions: inches, unless otherwise specified.
2. BSC = Basic lead spacing between centers.
3. Dimensions D and E1 do not include mold flash protrusions and should be measured from the bottom of the package.
4. Formed leads shall be planar with respect to one another within. 0004 inches at the seating plane.

## 13.2 8-Pin PDIP 300-mil



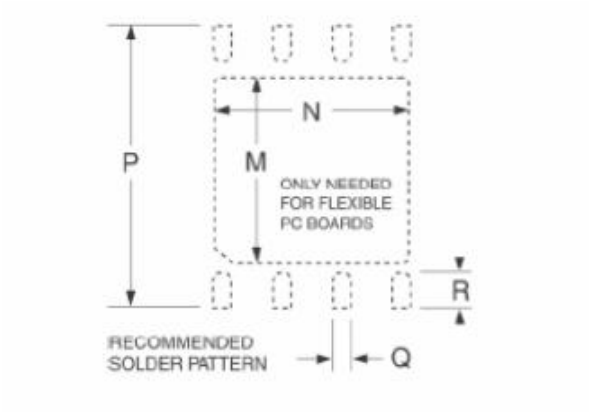

| SYMBOL | Dimension in inch | | | Dimension in min | | |
|---|---|---|---|---|---|---|
| | MIN | Nom | MAX | MIN | Nom | MAX |
| A | --- | --- | 0.210 | --- | --- | 5.334 |
| $A_1$ | 0.015 | --- | --- | 0.381 | --- | --- |
| $A_2$ | 0.125 | 0.130 | 0.135 | 3.18 | 3.30 | 3.43 |
| B | 0.016 | 0.018 | 0.022 | 0.41 | 0.46 | 0.56 |
| $B_1$ | 0.058 | 0.060 | 0.064 | 1.47 | 1.52 | 1.63 |
| c | 0.008 | 0.010 | 0.014 | 0.20 | 0.25 | 0.36 |
| D | 0.360 | 0.365 | 0.370 | 9.14 | 9.27 | 9.40 |
| E | 0.290 | 0.300 | 0.310 | 7.37 | 7.62 | 7.87 |
| $E_1$ | 0.245 | 0.250 | 0.255 | 6.22 | 6.35 | 6.48 |
| $e_1$ | 0.090 | 0.100 | 0.110 | 2.29 | 2.54 | 2.79 |
| L | 0.120 | 0.130 | 0.140 | 3.05 | 3.30 | 3.56 |
| α | 0 | --- | 15 | 0 | --- | 15 |
| e A | 0.335 | 0.355 | 0.375 | 8.51 | 9.02 | 9.53 |
| S | --- | --- | 0.045 | --- | --- | 1.14 |

## 13.3 8-contact 6x5 WSON




| SYMBOL | MILLIMETERS | | | INCHES | | |
|---|---|---|---|---|---|---|
| | MIN | TYP. | MAX | MIN | TYP. | MAX |
| A | 0.70 | 0.75 | 0.80 | 0.0276 | 0.0295 | 0.0315 |
| A1 | 0.00 | 0.02 | 0.05 | 0.0000 | 0.0008 | 0.0019 |
| A2 | | 0.55 | | | 0.0126 | |
| A3 | 0.19 | 0.20 | 0.25 | 0.0075 | 0.0080 | 0.0098 |
| b | 0.36 | 0.40 | 0.48 | 0.0138 | 0.0157 | 0.0190 |
| D(3) | 5.90 | 6.00 | 6.10 | 0.2320 | 0.2360 | 0.2400 |
| D1 | 3.30 | 3.40 | 3.50 | 0.1299 | 0.1338 | 0.1377 |
| E | 4.90 | 5.00 | 5.10 | 0.1930 | 0.1970 | 0.2010 |
| E1(3) | 4.20 | 4.30 | 4.40 | 0.1653 | 0.1692 | 0.1732 |
| e(2) | 1.27 BSC | | | 0.0500 BSC | | |
| K | 0.20 | | | 0.0080 | | |
| L | 0.50 | 0.60 | 0.75 | 0.0197 | 0.0236 | 0.0295 |

## 13.4 8-contact 6x5 WSON Cont'd.

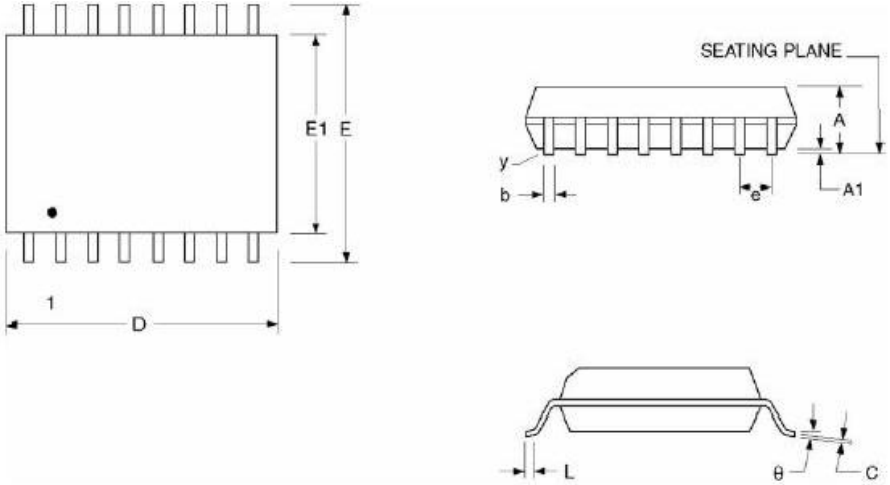



| SYMBOL | MILLIMETERS | | | INCHES | | |
|---|---|---|---|---|---|---|
| | MIN | TYP. | MAX | MIN | TYP. | MAX |
| SOLDER PATTERN | | | | | | |
| M | | 3.40 | | | 0.1338 | |
| N | | 4.30 | | | 0.1692 | |
| P | | 6.00 | | | 0.2360 | |
| Q | | 0.50 | | | 0.0196 | |
| R | | 0.75 | | | 0.0255 | |

**Notes:**

1. Advanced Packaging Information; please contact FIDELIX SEMICONDUCTOR for the latest minimum and maximum specifications.
2. BSC = Basic lead spacing between centers.
3. Dimensions D and E1 do not include mold flash protrusions and should be measured from the bottom of the package.
4. The metal pad area on the bottom center of the package is connected to the device ground (GND pin). Avoid placement of exposed PCB bias under the pad.

### 13.5 16-Pin SOIC 300-mil




| SYMBOL | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | 2.36 | 2.64 | 0.093 | 0.104 |
| A1 | 0.10 | 0.30 | 0.005 | 0.012 |
| b | 0.33 | 0.51 | 0.013 | 0.020 |
| C | 0.18 | 0.28 | 0.007 | 0.000 |
| D(3) | 10.08 | 10.49 | 0.397 | 0.413 |
| E | 10.01 | 10.64 | 0.394 | 0.419 |
| E1(3) | 7.39 | 7.59 | 0.291 | 0.299 |
| e(2) | 1.27BSC | | 0.050 | |
| L | 0.39 | 1.27 | 0.015 | 0.050 |
| θ | 0° | 8° | 0° | 8° |
| y | --- | 0.076 | --- | 0.003 |

**Notes:**

1. Controlling dimensions: inches, unless otherwise specified.
2. BSC = Basic lead spacing between centers.
3. Dimensions D and E1 do not include mold flash protrusions and should be measured from the bottom of the package.

## 14. ORDERING INFORMATION[1]

**FM XXXXXX - XXXXX X**

**Fidelix Memory**

**Product Family**
25 : SPI

**Organization**
S : Standard
D : Dual
Q : Quad

**Device Depth**
04 : 4M
08 : 8M
16 : 16M
32 : 32M
64 : 64M
4A : 128M

**Generation**
A : 1st
B : 2nd
C : 3nd

**Speed**
85 : 85MHz
1A : 104MHz

**Packing Type**
T : Tube (Standard)
R : Tape and Reel
Y : Tray
* Package NO Marking

**Business Package Type**
1 : 8 Pin 208 mil SOIC
2 : 16 Pin 300 mil SOIC
3 : 8 Pin 300 mil PDIP
4 : 8 Contact 6x5 WSON
5 : 8 Pin 150 mil SOIC
6 : 8 Contact 6x8 WSON
W : Wafer

**Core / IO Voltage**
A : 3.0V / 3.0V
B : 1.8V / 1.8V

**Temperature**
I (Industrial) : -40℃~85℃
C (Commercial) : 0℃~70℃